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***Journal of Scientific and Engineering Research*, 2017, 4(6):65-70**


**Research Article**

**ISSN: 2394-2630**
**CODEN(USA): JSERBR**

# Design & Analysis of on Chip Voltage Regulator Circuits for Low Power VLSI Applications

**Vijendra K Maurya[1], Navneet Agrawal[2], Ashik Hussan[3]**

[1]PhD Scholar, Department of Electronics & Communication Engineering, Career Point University, Kota, Rajasthan, India. maurya.vijendra@gmail.com
[2]Professor, College of Technology and Engineering, Maharana Pratap University of Agriculture and Technology, Udaipur, Rajasthan, India. navneetctae@gmail.com
[3]Head, Department of Computer Science & Engineering, Engineering Career Point University, Kota, Rajasthan, India. ashik.hussain@cpur.edu.in

**Abstract** Due to advancement of Digital India a lot of peoples move to digital era. Today Life cannot be seemed possible without electronic gadgets. Regarding portability power dissipation is main constraint. Consumer demands more features in small size and extended battery life at a lower cost On chip voltage regulator is widely used in integrated circuits (ICs) due to the continuous power supply reduction which is dedicated to several kind of applications Cameras (CMOS image sensor), LCD Display, Protection Device, Battery-powered Devices, Smoke Detectors, $CO_2$ Detectors etc. On chip voltage regulator used in this application, basically it is DC to DC converter which has capacitor instead of an inductor or transformer for energy storage. In this paper comparison established between two techniques of on chip voltage regulator circuits i.e. Feed -Forward Ripple Cancellation (FFRC) and MOS Capacitor Compensation (MCC) techniques in terms output voltage, power consumption, load current, drop out voltage and load regulation.

**Keywords** voltage regulator, load current, load regulation

## 1. Basic of Voltage Regulator

The system which is battery-operated, low Drop-out CMOS design becomes necessary for low power dissipation. CMOS processes have been used in large-scale integrated circuits like LSI and microprocessors, they have been miniaturized constantly. Advantage of the miniaturization technology, CMOS linear regulators has become the power management ICs that are widely used in portable electronics products to realize low profile, low dropout, and low supply current. Therefore voltage regulator circuit is likely to become a crucial component in low power CMOS design.

### 1.1. Low Drop-out Voltage Regulator

LDO voltage regulators are necessary building blocks in power-management systems. Power management systems for microprocessors and portable devices often use multiple LDO regulators to offer a regulated supply voltage with minimum ripple to supply-noise-sensitive blocks [1]. To raise battery-life and to achieve better power efficiency, low-dropout regulators are essential. The low drop-out nature of the regulator makes it appropriate for use in many applications, namely, automotive, portable and biomedical applications. LDO (Low Dropout) regulators enable battery to be used up to the limit, and therefore the regulators are now essential power management ICs for the devices like mobile phones, digital cameras, and laptop PCs to have long battery life. Because LDO regulators feature to pull large current with small input-output voltage

differential while minimizing heat losses, they can meet the wide range of current requirements of each device. In linear regulators, the output voltage is affected by the input voltage. LDO regulator is a DC linear voltage regulator that can regulate the output voltage even when the supply voltage is very close to the output voltage. The advantages of a low dropout voltage regulator over other DC to DC regulators include the absence of switching noise, smaller device size, and greater design simplicity. A significant disadvantage is that, unlike switching regulators, linear DC regulators must dissipate power across the regulation device in order to regulate the output voltage. It offers an optimal combination of low dropout voltage, low quiescent current, fast transient response, low noise and good ripple rejection.

LDO voltage regulator is a circuit which is designed to provide a pre-determined DC voltage under varying load, temperature and input voltage condition. The main components are a power FET and a differential amplifier (error amplifier). One input of the differential amplifier observes the fraction of the output determined by the resistor ratio of R1 and R2. The second input to the differential amplifier is from a stable voltage reference. If the output voltage rises too high relative to the reference voltage, the drive to the power FET changes to maintain a constant output voltage. A variety of electronic equipments contain circuit which convert AC supply voltage into DC voltage at the desired level.

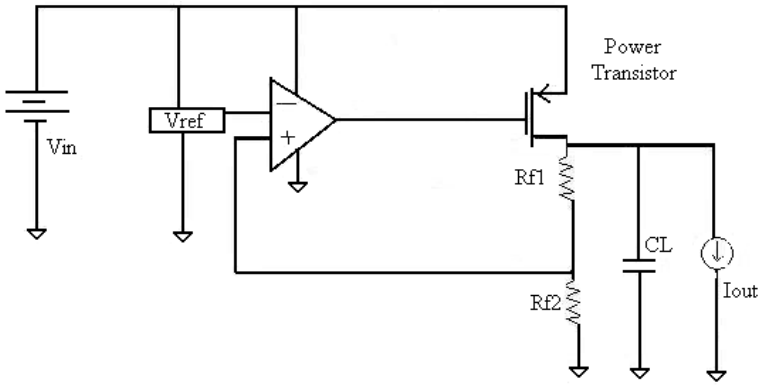


*Figure 1.1: LDO Voltage Regulator Circuit (1)*

The DC voltage attained from such circuits must be stable. The DC voltage regulated power supplies are used to acquire the stable DC voltage yet there are variations in load current, temperature and AC line voltage. This power supply attenuates the ripple in the input voltage. The essential function of a voltage regulator is voltage regulation, provides clean, constant, accurate voltage to a circuit. LDO consists of a pass transistor, an error amplifier EA, a feedback network (RF1 and RF2) and a immense off chip capacitor .$C_L$ represent Current source, $I_L$ represents the required current by the load.

## 2. Component of On Chip Voltage Regulator

### 2.1. Reference Voltage

In the reference voltage generator, a zener diode is being compelled to operate at fixed point (so that zener output voltage is a fixed voltage) by a constant current Source which comes along with an amplifier to generate a constant voltage of 7.15V at the Vref pin of the IC.

### 2.2. Error Amplifier

An error amplifier is most commonly encountered in feedback unidirectional voltage control circuits, where the sampled output voltage of the circuit under control, is feedback and compared to a stable reference voltage. Any difference between the two voltage generates a compensating error voltage which tends to move the output voltage towards the design specification. An error amplifier, it amplifies an error signal. This error is based on the difference between a reference signal and the input signal.

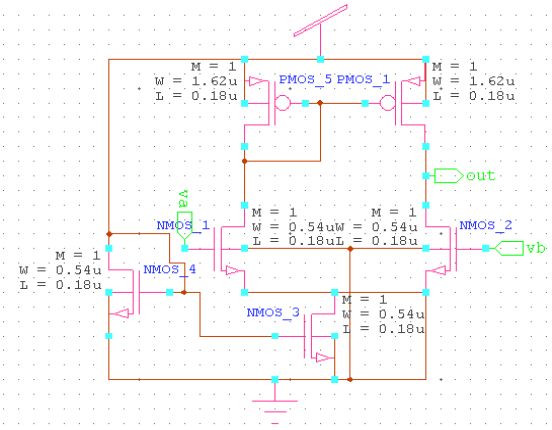


*Figure 2.1: Error amplifier circuit [3]*

This error amplifier which is used in regulated power supplies, D.C. power amplifier, measurement equipment etc.

### 2.3. Pass Device

This device must be able to handle the maximum load current without causing over temperature and reliability issues. The pass device is a PMOS transistor. However, a variety of pass devices are available, and LDOs can be classified depending on which type of pass device is used.

### 2.4. Feedback resistors

In electronics, a voltage divider is a simple linear circuit that generates an output voltage ($V_{out}$) that is a fraction of its input voltage ($V_{in}$). Voltage division refers to the partitioning of a voltage among the components of the divider.

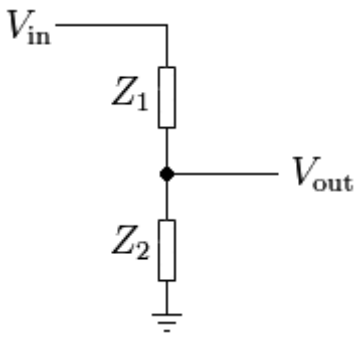


*Figure 2.2: Feedback Resistors structure [4]*

The input voltage is applied across the series impedances $Z_1$ and $Z_2$ and the output is the voltage across $Z_2$. Applying Ohm's Law, the relationship between the input voltage $V_{in}$ and the output voltage $V_{out}$ can be found:

$$Vout = \left(\frac{Z2}{Z1 + Z2}\right) Vin$$

## 3. Circuit Implementation

**3.1 LDO voltage regulator using feed-forward ripple cancellation (FFRC) technique:**-This technique gets a high power supply rejection (PSR) over a wide frequency range. To eliminate input ripples from appearing at the output, a zero transfer gain is necessary from the input to the output in Fig.3.1 This is achieved by implementing a feed-forward path that reproduces same input ripples at the gate of the pass transistor Mp. Hence, the gate-overdrive voltage is independent of input ripples and as a result no ripple appears across the

load. Figure. 3.1 presents a simplified block-level description of the FFRC-LDO and actual case, part of the ripples leak through the finite output resistance of Mp and must be removed.

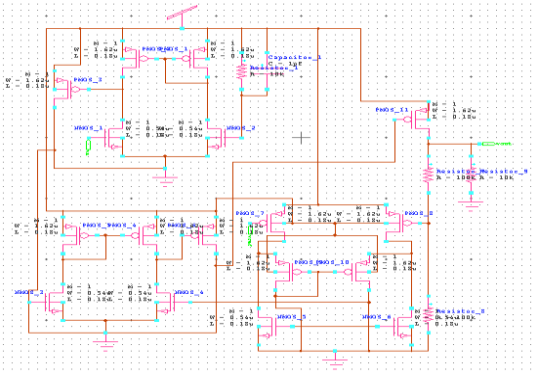

*Figure 3.1: Schematic of Feed-Forward Ripple Cancellation Technique*

**3.2. MOS Capacitor Compensation Technique [MCC] using single stage amplifier**

This technique present a full on-chip and area efficient low-dropout voltage regulator (LDO) which use the technique nested miller compensation with active capacitor (NMCAC) to eliminate the external capacitor without compromising the stability of the system in the full output current range. The external capacitor is removed allowing for greater power system integration for system on-chip applications. To have a fast transient response, a buffer is inserted between the error amplifier and the power MOS transistor. This technique reduces the dc loop gain in the low supply voltage. To achieve a large dc loop gain, a gain stage replaces this buffer in the regulator. It converts the LDO to be a multi-stage amplifier. To stabilize a multi-stage LDO, the complicated frequency compensation is needed

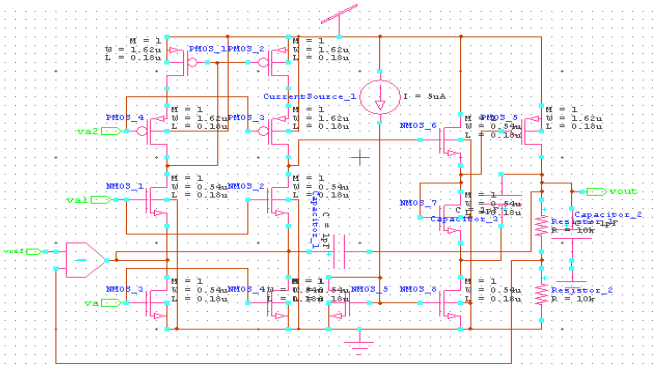


*Figure 3.2: Schematic of MOS Capacitor Compensation Technique [MCC] using single stage amplifier*

**4. Result, Analysis and Comparison**

In this section we have compared the result of Feed-Forward Ripple Cancellation Technique (FFRC) and MOS Capacitor Compensation Technique [MCC] using single stage amplifier techniques on chip voltage regulator circuits. Here we show that the Simulation results of both types of voltage regulator. Function of designs is verified by using simulation based verification. This verification guarantee that the design is functionally correct when tested with given inputs. Designed voltage regulator pump have been implemented and simulated on Tanner tool in 180 nm technology.

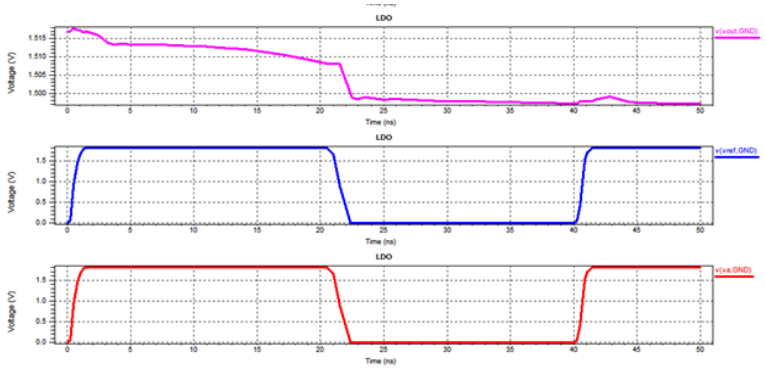

*Figure 4.1: output waveform of feed-forward Ripple cancellation technique*

**Table 4.1:** output voltage, load current, power consumption, dropout voltage, load regulation at different $V_{DD}$ of FFRC

| Input(V) | Output(V) | Power Consumption(mW) | Load Current($\mu$A) | Drop-Out Voltage (V) | Load Regulation (V/mA) |
|---|---|---|---|---|---|
| 1.5 | 1.23 | 0.654 | 52 | 0.27 | 6.3 |
| 1.8 | 1.52 | 0.623 | 72 | 0.28 | 7.0 |
| 2.0 | 1.7 | 0.386 | 88 | .30 | 8.01 |

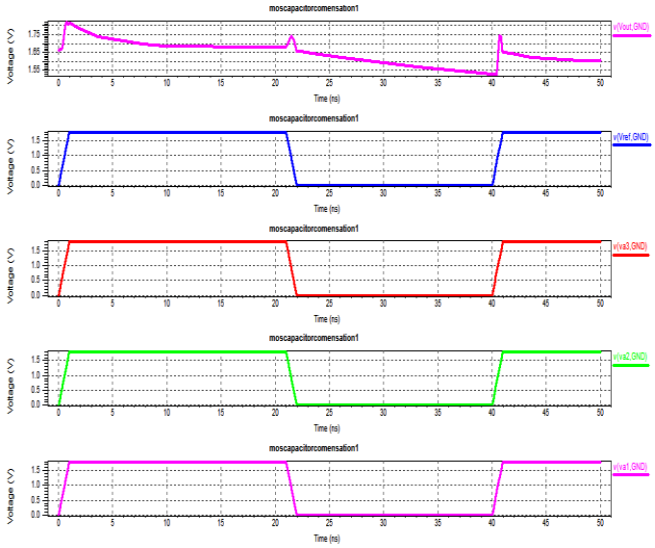

*Figure 4.2: output waveform of MOS capacitor compensation technique using single stage operational amplifier*

**Table 4.2:** output voltage, load current, power consumption, dropout voltage, load regulation at different $V_{DD}$ of MCC

| Input (V) | Output (V) | Power Consumption(mW) | Load Current ($\mu$A) | Drop-Out Voltage (V) | Load Regulation (V/mA) |
|---|---|---|---|---|---|
| 1.5 | 1.45 | 0.439 | 5 | 0.05 | 1.56 |
| 1.8 | 1.75 | 0.791 | 10 | 0.05 | 2..93 |
| 2.0 | 1.95 | 1.08 | 20 | 0.05 | 3.68 |

## 5. Conclusion

From the above results, it was concluded that at same input voltage output voltage of MCC on chip voltage regulator is higher than FFRC on chip voltage regulator with less power consumption. Drop output voltage of MCC is constant while FFRC output voltage is variable with supply voltge.

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