Available online www.jsaer.com

Journal of Scientific and Engineering Research, 2017, 4(1):172-183

ISSN: 2394-2630
CODEN(USA): JSERBR

Research Article

An efficient unified power flow controller design with binary programmed PWM

Muhammad Aashir*, Syed S.H. Shah, Faraz Sawati, Muhammad T. Kiyani

Department of Electrical Engineering, COMSATS Institute of Information Technology, Wah-47040, Pakistan

Abstract This article presents an energy efficient implementation of a digital nonlinear feedback compensated Unified Power Flow Controller (UPFC) and its application to the power flow control. The proposed design incorporates generation of the Binary Programmed Pulse Width Modulation (BPPWM) sequences. These sequences are then used as the gate drive signals that are optimal for the selective harmonic elimination from the output voltage, maximization of the fundamental component and resulting in an efficient electronic circuit design as compared to the traditional gate drive techniques in terms of the switching losses and the filtering energy losses. The generation of BPPWM sequences is addressed as a Mixed-Integer Linear Programming (MILP) problem. The UPFC realization is followed by a multi-loop compensator design for the load voltage amplitude regulation and power factor tracking for power flow control. The proposed control algorithm incorporates feedback linearization and digital saturated Proportional-Integral-Derivative (PID) action. The simulation results of the control algorithm are presented. The experimental validation of theoretically proposed controller is also presented by implementing the discrete time realization of control algorithm using digital controller interfaced in real time with MATLAB®/Simulink® in Rapid Control Prototyping Mode (RCP) of operation. The feasibility of the proposed design is theoretically and experimentally verified by its efficiency comparison with the classical techniques and satisfactorily stable closed loop responses.

Keywords Rapid Control Prototyping, Voltage Source Converter, Inverter, Mixed-Integer Linear Programming.

1. Introduction

The Unified Power Flow Controller (UPFC) is one of the most significant solid state Flexible Alternating Current Transmission Systems (FACTS) device and comprises of a Static Synchronous Compensator (STATCOM) and a Static Synchronous Series Compensator (SSSC) coupled via a common DC bus [1-2]. It is 3 degrees of freedom device, which integrating the voltage, active power and reactive power regulation in a four-quadrant operation. It has many applications, for instance, flexible power flow control, damping power system oscillations to improve transient stability, emergency power support to avoid power blackout, power factor compensation, improvement of transmission capability and reduction of transmission cost [3-4]. A typical UPFC consists of a series and a shunt voltage source converter (VSC). The shunt converter is energized by a booster shunt transformer and it provides power to a DC bus. The shunt converter can be three phase or single phase and it is typically implemented as a full bridge controlled converter [5]. The series inverter injects a series voltage in phase lines for power flow control and voltage regulation. Various gate drive techniques are implemented for series inverter operation, for instance, a comprehensive description is presented in [6-7]. A Custom Programmed PWM (CPPWM) technique is proposed in [8]. As the first objective of this article, we have implemented Binary Programmed PWM (BPPWM) technique to generate gate drive sequences and it is shown that this technique proves to be more energy efficient than traditional techniques like the Sinusoidal PWM (SPWM) scheme and CPPWM scheme proposed in [8] The generated BBPWM sequences are decomposed for the inverter topology that does not require multiple isolation supplies for gate drives of three phase lines. The second objective of our article is the regulation of the load voltage and control of the power flow in terms of power factor tracking. Various control techniques are implemented in literature, for instance, continuous time PI (proportional-integral) controller and linear quadratic tracker, robust adaptive fuzzy control algorithm etc. [9-11] . We have proposed discrete control algorithm that incorporates feedback linearization and discrete saturated PID action. This algorithm is simple and has ease of implementation as compared with other techniques in literature such as LQR and fuzzy adaptive techniques. The control algorithm is simulated and implemented on the digital controller for experimental testing. The results show satisfactorily stable operation for the power factor reference tracking and the load voltage regulation.

2. Overview of the Proposed UPFC System

Figure 1 shows the load side voltage injection mode UPFC configuration that has been implemented in this article. The DC link is energized by a Phase A shunt VSC. The voltage and the power flows are controlled in the three phases by three BPPWM series VSC coupled to the common DC link. Figure 2 illustrates the proposed control strategy for the UPFC. Two separate control loops are implemented to control supply power factor and load voltage amplitude. Figure 3 gives an expanded view of Figure 2 for implementation of the UPFC hardware setup. The inverter part and the variable DC supply part are the same as implemented in [8].

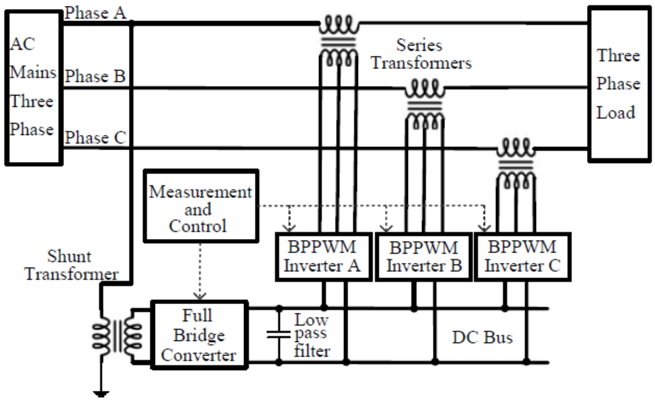

Figure 1: The load-side voltage injection BPPWM UPFC configuration

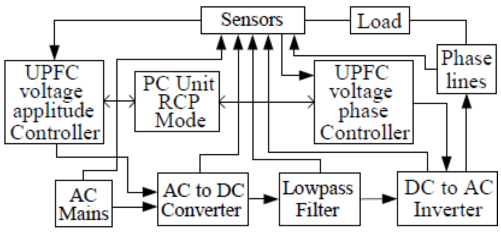

Figure 2: The proposed control strategy for UPFC

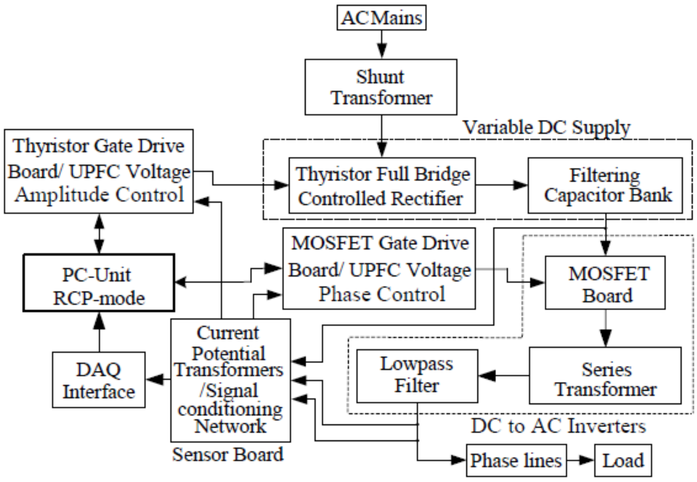

Figure 3: An expanded view of UPFC hardware setup

3. The Binary Programmed PWM Generation Problem

The BPPWM problem involves generation of a binary sequence, such that if this sequence is used as a gate drive signal for the inverter MOSFET board in Figure 3 then the output of the inverter has desired fundamental amplitude and desired harmonic contents. The BPPWM sequence is selected to have the quarter wave symmetry, hence we need to design the sequence for interval $[0, \pi / 2]$ and extend it accordingly. The quarter wave interval is subdivided into N bins for the BPPWM sequence as shown in Figure 4. We have to select a binary value f_k for each bin such the resulting binary sequence has maximum fundamental component and selected harmonic contents removed or minimized in its Fourier spectrum.

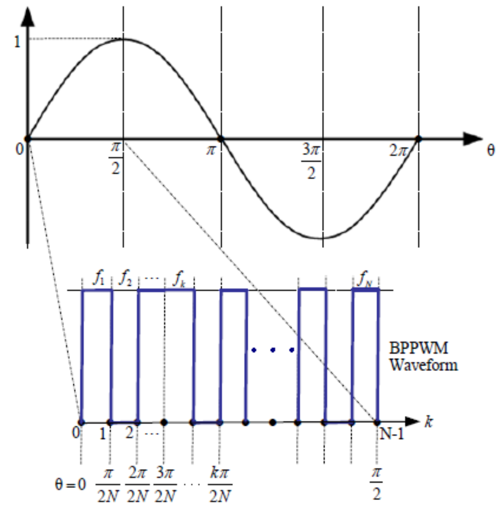

Figure 4: A general quarter-wave symmetric BPPWM sequence

The harmonic contents of BPPWM sequence are given by Equation 1, with $f(\theta) = f_k \in \{0,1\}$ and $n \in \{1,3,5,\cdots\}$.

$$b_n = \frac{4}{\pi}\int_0^{\pi/2} f(\theta)\sin(n\theta)d\theta = \frac{4}{n\pi}\sum_{k=0}^{N-1} f_k C(k,n),$$
$$C(k,n) = \cos\left(\frac{kn\pi}{2N}\right) - \cos\left(\frac{(k+1)\,n\,\pi}{2N}\right) \tag{1}$$

The BPPWM sequence generation problem can be formulized as a Mixed-Integer Linear Programming (MILP) optimization problem given by Equation 2.

$$\max_{f_k} b_1 = \frac{4}{\pi}\sum_{k=0}^{N-1} f_k C(k,1) \text{ s.t. } \begin{cases} b_n = \dfrac{4}{\pi}\displaystyle\sum_{k=0}^{N-1} f_k C(k,n) = 0 \\ f_k \in \{0,1\} \end{cases} \tag{2}$$

We have selected to eliminate first 16 odd harmonics with N=55. The equality constraints in Equation 2 can now be written in matrix notation Equation 3.

$$\begin{bmatrix} c(0,3)/3 & c(1,3)/3 & \cdots & c(54,3)/3 \\ c(0,5)/5 & c(1,5)/5 & \cdots & c(54,5)/5 \\ \vdots & \vdots & \ddots & \\ c(0,31)/31 & c(1,31)/31 & \cdots & c(54,31)/31 \end{bmatrix} \begin{bmatrix} f_0 \\ f_1 \\ \vdots \\ f_{54} \end{bmatrix} = \mathbf{0} \tag{3}$$

The problem in Equation 2 is solved by using the MILP solver in MATLAB. The resulting sequence is given by Equation 4.

$$f_k = \{000000110000000011011111011111111111111111111111111111111111\} \tag{4}$$

The sequence in Equation 4 can be extended to generate complete cycle of the BPPWM waveform as shown in Figure 5.

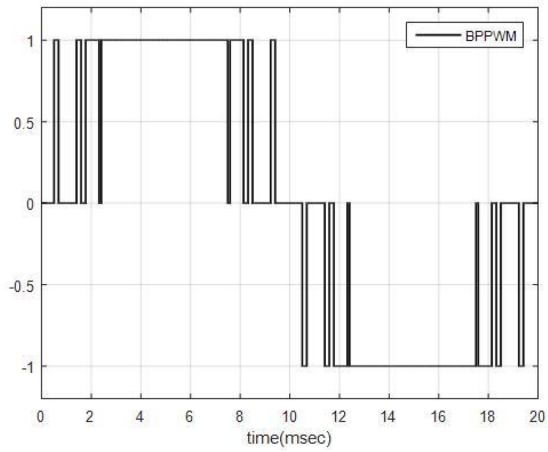

Figure 5: A complete single cycle of BPPWM sequence

The amplitude of normalized harmonic components of BPPWM are plotted and compared with the harmonic contents of Sinusoidal PWM (SPWM) and CPPWM in Figure 6.

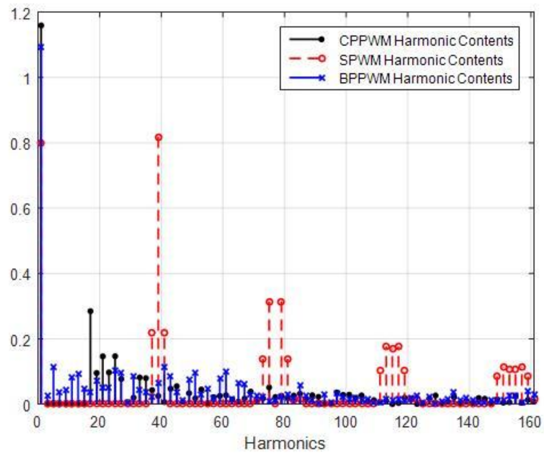

Figure 6: The harmonic contents of different PWM schemes

The fundamental component of BPPWM is comparable to CPPWM and greater than SPWM. The integral constraints have resulted in a BPPWM sequence with small non-zero amplitudes of first 16 harmonics as compared to the other schemes. The amplitude of the harmonic contents in BPPWM are smaller and equally spread as compared to SPWM.

4. The Power Efficiency Considerations for BPPWM Scheme

4.1. The Running Switching Energy Loss (RSEL)

The Running Switching Energy Loss (RSEL) [8] is defined in Equation 5.

$$e_{rsel}(t) = \int_0^t p_s(t)d\tau \tag{5}$$

RSEL is used to compare energy and power efficiency of different PWM schemes. RSEL is plotted in Figure 7 for a single cycle of various PWM schemes. For any given cycle, the BPPWM scheme has 44% and 13% less loss as compared to SPWM and CPPWM schemes respectively.

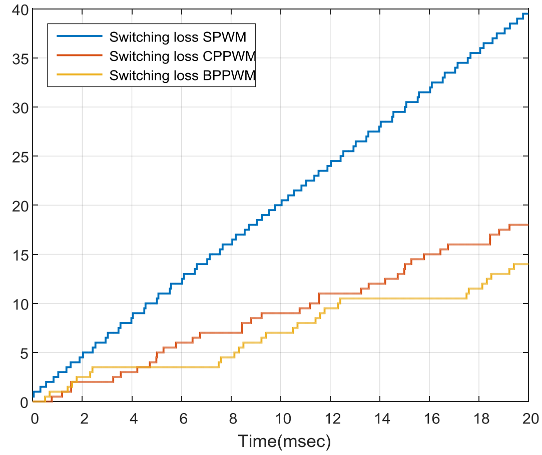

Figure 7: The running Switching Energy Loss for various PWM schemes

4.2. The Receding Harmonic Energy Loss (RHEL)

The Receding Harmonic Energy Loss (RHEL) in Equation 6 defined in [8] as a comparison criteria for energy and power efficiency for different PWM schemes.

$$E_{h_x}[n_i] = \sum_{k=n_i}^{n_N} \left(h_x[k]\right)^2 \tag{6}$$

RHEL is plotted in Figure 8 for a single cycle of various PWM schemes. If a filter is chosen with a cutoff frequency $f_c \in (10 f_F, 20 f_F)$,where f_F is the fundamental frequency, then it is evident from Figure 8 that the BPPWM scheme has 83% and 20% less filtering loss as compared to the SPWM and CPPWM schemes respectively.

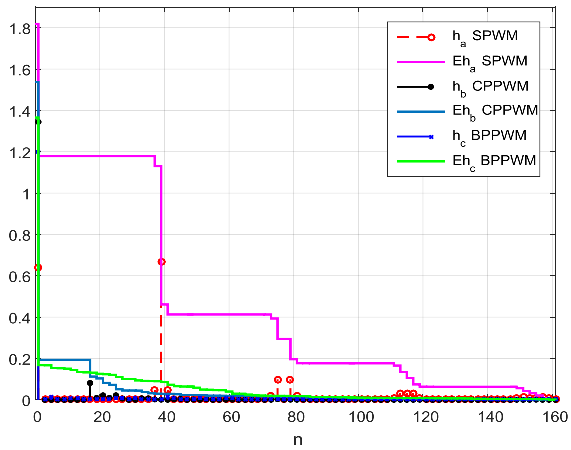

Figure 8: RHEL for various PWM schemes

5. Multiloop Compensator Design for UPFC

The circuit layout of the single phase UPFC is shown in Figure 9. The first objective is to regulate load voltage amplitude V_L by adjusting V_c . The second objective is to track source side power factor or equivalently θ_{is1} by adjusting θ_{vc} .

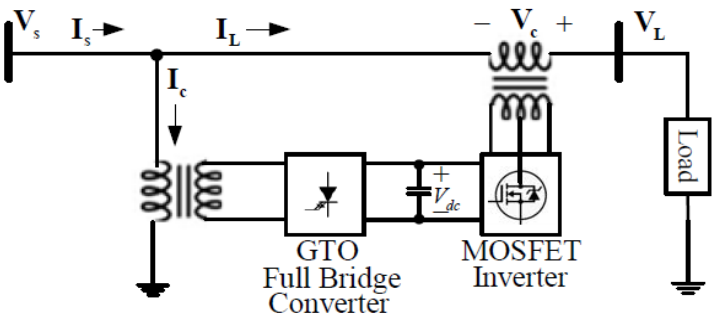

Figure 9: A single phase UPFC model

5.1. The Steady State Model of Proposed UPFC

The fundamental component of supply current is Figure 9 is given by Equation 7.

$$\begin{aligned}\mathbf{I}_{s1} &= I_{s1}\angle\theta_{is1} = \mathbf{I}_c + \mathbf{I}_L = I_c\angle\theta_{ic} + I_L\angle\theta_{iL}\\ &= \left(I_c\cos(\theta_{ic}) + \frac{V_s}{Z_L}\cos\theta_{zL} + \frac{V_c}{Z_L}\cos\left(\theta_{vc}-\theta_{zL}\right)\right)\\ &\quad + j\left(I_c\sin(\theta_{ic}) - \frac{V_s}{Z_L}\sin\theta_{zL} + \frac{V_c}{Z_L}\sin\left(\theta_{vc}-\theta_{zL}\right)\right)\end{aligned} \tag{7}$$

Using Equation 7 we get,

$$\cos\theta_{is1} = \frac{I_c}{I_{s1}}\cos(\theta_{ic}) + \frac{V_s}{Z_L I_{s1}}\cos\theta_{zL} + \frac{V_c}{Z_L I_{s1}}\cos\left(\theta_{vc}-\theta_{zL}\right) \tag{8}$$

The phasor diagram of UPFC is shown in the Figure 10.

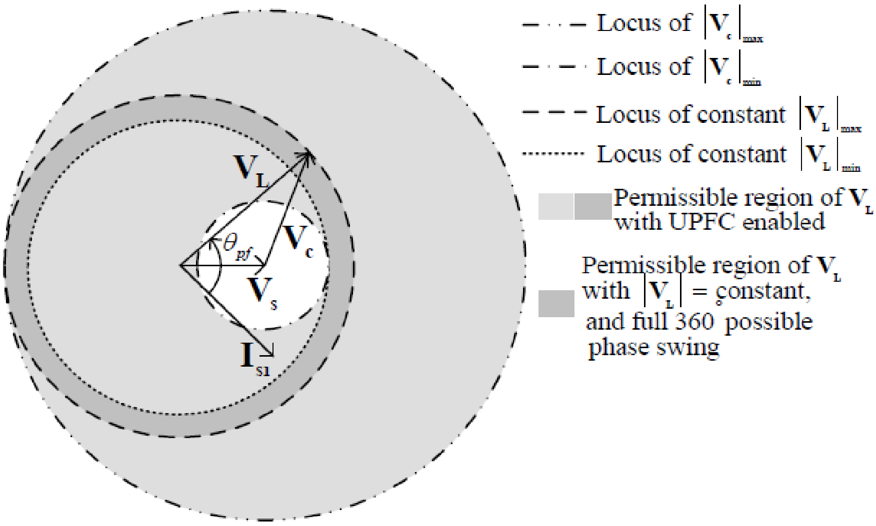

Figure 10: The single Phase UPFC phasor diagram

Using Equation 7 and Equation 8, the source side power factor (p.f.) is given by Equation 9.

$$\begin{aligned}\mathrm{pf} &= \cos(\theta_{vs}-\theta_{is1}) = f_1 + (\cos(\theta_{vc}-\theta_{zL}))V_c/Z_L I_{s1},\\ f_1 &= (I_c/I_{s1})\cos(\theta_{ic}) + (V_c/Z_L I_{s1})\cos\theta_{zL}\end{aligned} \tag{9}$$

Using sine law in Figure 10, we get,

$$V_{L,RMS} = -\sin(\theta_{vc})V_c / (\sqrt{2}\sin(\theta_{vL})) \tag{10}$$

Equation 9 and Equation 10 present the steady state (SS) model for UPFC based source side power factor and RMS load voltage respectively.

5.2. Feedback Linearization for Steady State UPFC Model

The measured variables for our UPFC system are $\mathbf{I_c}, \mathbf{I_L}, \mathbf{I_{s1}}, \mathbf{V_c}, \mathbf{V_s}, \mathbf{V_L}$ and $\mathbf{Z_L} = \left(V_L / I_L \right) \angle \theta_{vL} - \theta_{iL}$. The power factor and the RMS load voltage SS models Equation 8 and Equation 9 are nonlinear with respect to the inputs θ_{vc} and V_c respectively. The feedback linearization is applied using the measured variables and it results in manipulated variables given by Equation 11.

$$U_{\theta pf} = \frac{Z_L I_{s1}}{V_c} \cos^{-1}\left(\theta_{vc} + \theta_{zL}\right) - f_1, \;\; U_V(s) = \frac{\sqrt{2}\sin\theta_{vL}}{-\sin\theta_{vc}} V_c \tag{11}$$

5.3. The Transient Model of Proposed UPFC

The transient model of UPFC is given by Equation 12. This model is obtained by system identification technique using step signal excitation in Figures 11 through 14.

$$\begin{aligned}
V_{L,RMS}(s) &= \frac{1.98\times10^{12}}{D_1(s)} U_V(s) + \frac{-4.98\times10^{21}}{D_2(s)} U_{\theta pf}(s), \\
D_1(s) &= s^4 + 1005s^3 + 9.43\times10^5 s^2 + 3.96\times10^8 s \\
&\quad + 1.55\times10^{11}, \\
D_2(s) &= s^6 + 1244s^5 + 1\times10^6 s^4 + 5.4\times10^8 s^3 + 1.8\times10^{11} s^2 \\
&\quad + 2\times10^{13} s + 2\times10^{15} \\
PF(s) &= \frac{1660}{s^2 + 61.58s + 1934} U_V(s) \\
&\quad + \frac{-0.3621s + 12.07}{s^2 + 54.45s + 1755} U_{\theta pf}(s)
\end{aligned} \tag{12}$$

5.4. Compensator Design and Simulation

A multi-loop compensator design strategy has been implemented. One loop regulated load voltage and treats p.f fluctuations as disturbance. He other loop stabilizes p.f. and treats load voltage fluctuations as disturbance. The digital PID controller structure in Equation 13 is selected for either loop.

$$\mathrm{C(z)=K_p + K_i / b(z) + K_d N / (1+Nb(z))}, \;\; \mathrm{b(z)= T_s z / (z\text{-}1)} \tag{13}$$

The values of gains are tuned online by operating the plant in RCP mode. The voltage and p.f. controller gains are $K_p=0.2$, $K_i=1$, $K_d=3.5\times10^{-3}$ and $K_p=0.1$, $K_i=8\times10^{-6}$ $K_d=2\times10^{-4}$ respectively with $N=50$. The p.f. and load voltage controllers, as shown in Figure 15 and Figure 16 respectively, take measured variables and error signals as inputs. The feedback linearization is followed by the control algorithm in Equation 13 and the manipulated variable range transformations.

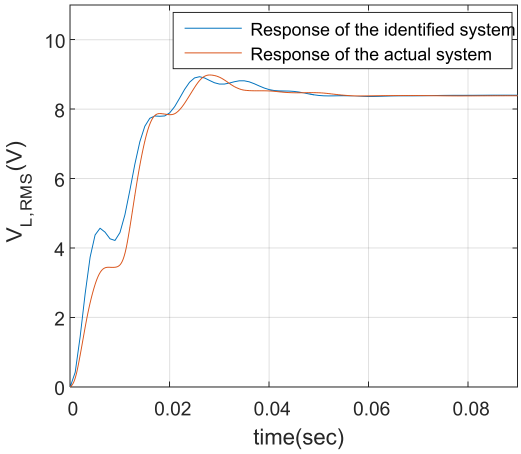

Figure 11: The response of RMS load voltage to unit step UPFC voltage

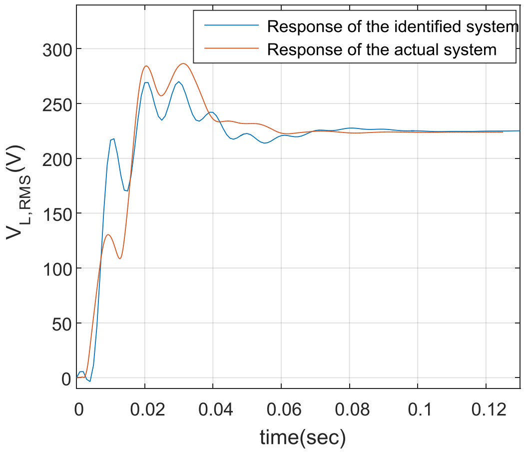

Figure 12: The response of RMS load voltage to unit step UPFC voltage phase

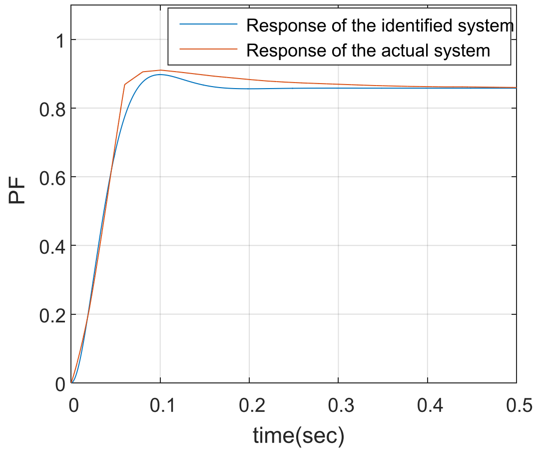

Figure 13: The response of P.F to unit step UPFC voltage phase

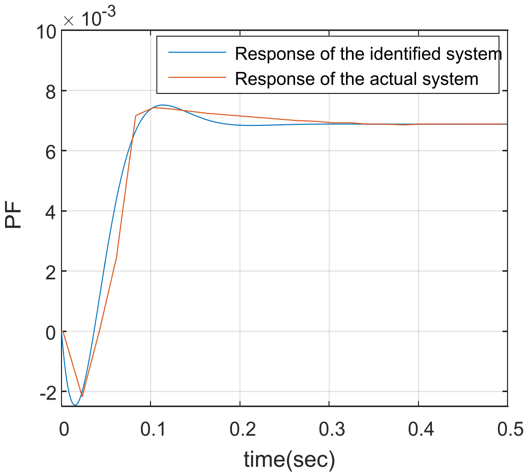

Figure 14: The response of P.F. to unit step UPFC voltage

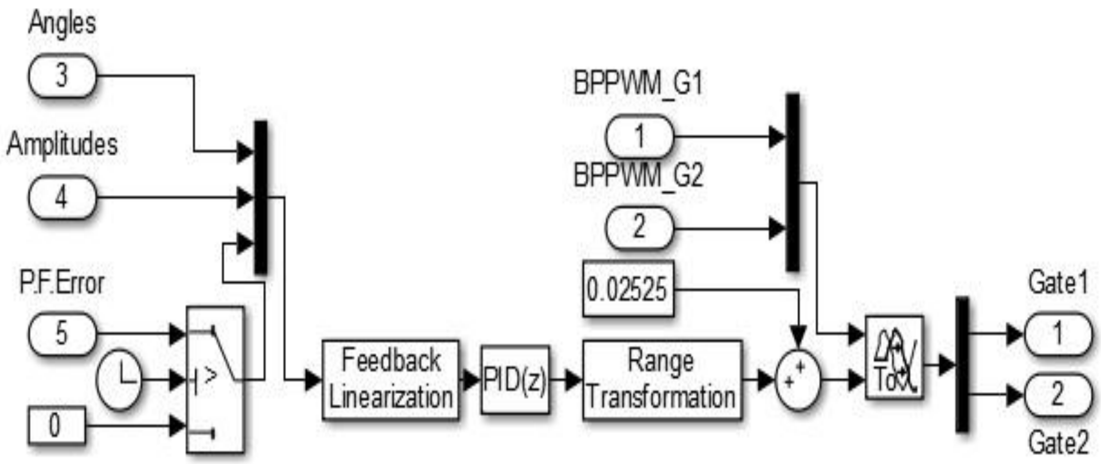

Figure 15: The power factor tracking controller

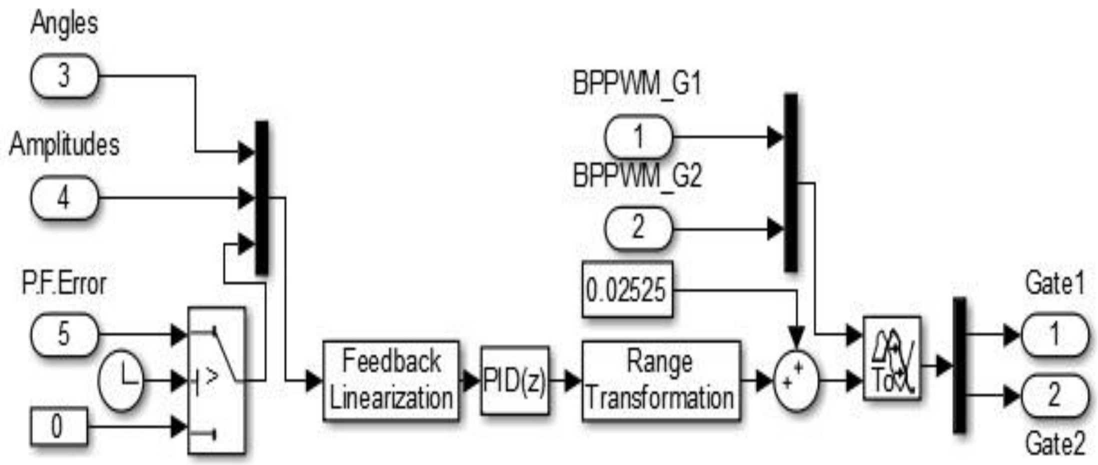

Figure 16: The RMS load voltage regulation controller

The closed loop p.f. tracking response is shown in Figure 17. The load voltage regulation response at 400Vrms is shown in Figure 18. Responses are stable with zero SS error.

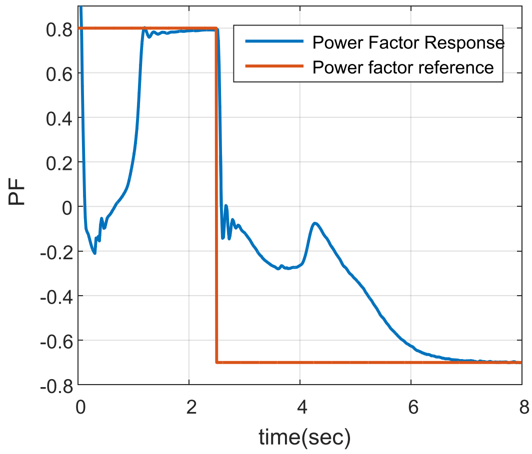

Figure 17: The closed loop p.f. tracking response

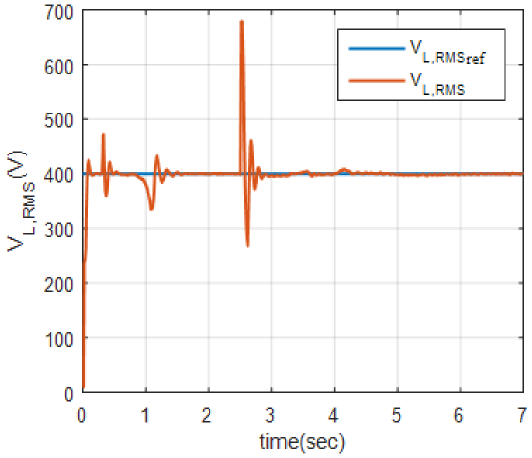

Figure 18: The load voltage regulation with p.f. disturbance at 2.5sec

6. Experimental Results

The experimental setup of Figure 19 is used to test and validate the efficiency of the BPPWM scheme and responses of the controller. Figure 20 shows the operation of the plant in RCP mode. This configuration is used to tune the controller gains for the load voltage regulation and the p.f. tracking. Figure 21 shows the actual 0.8 lag closed loop p.f. step response at 0.25sec. The response is stable with 2sec setting time and zero SS error. Figure 22 shows the experimental 400V closed loop RMS load voltage step response. The response is stable with 0.1sec setting time, zero SS error and withstands p.f. step change of Figure 21.

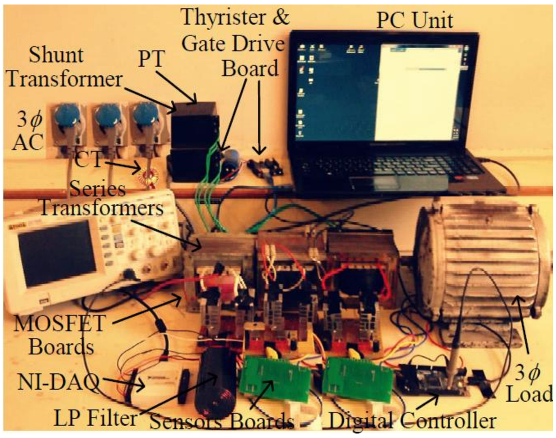

Figure 19: The experimental setup

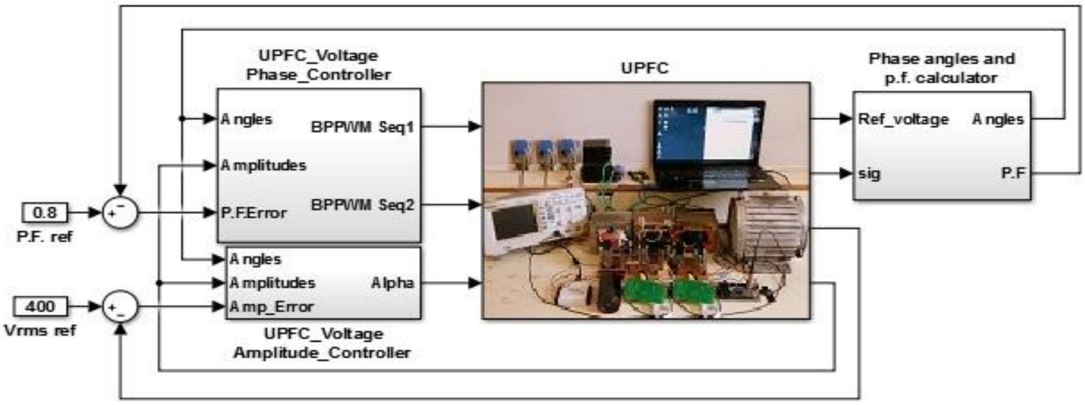

Figure 20: The RCP mode of operation for UPFC system controller tuning and experimental validation

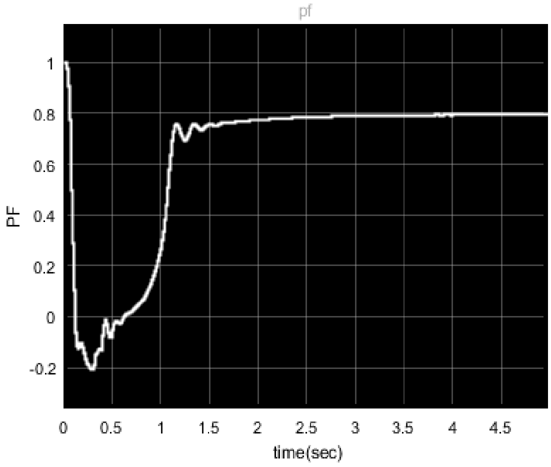

Figure 21: The experimental closed loop p.f. step response

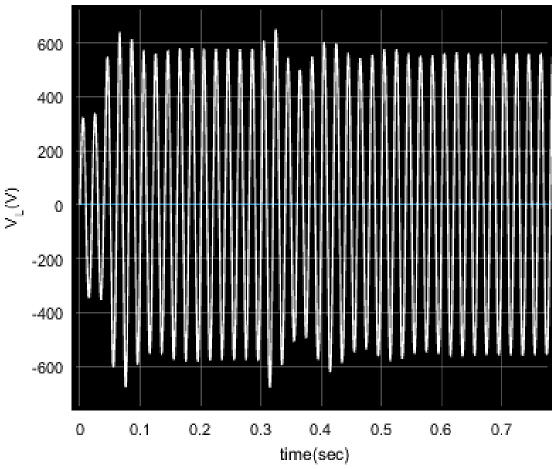

Figure 22: The experimental closed loop RMS load voltage step response with the p.f. step disturbance

7. Discussion and Conclusions

An energy efficient UPFC system has been presented with the feedback linearization and discrete PID controller algorithm to regulate the load voltage and maintain the active and reactive power flows by tracking the source power factor. A binary programmed PWM scheme has been implemented with the objective of selective harmonic elimination and maximization of the fundamental. As compared with a special case of SPWM and CPPWM schemes, our results show a promising 44% and 13% reduction in switching losses and 83% and 20% reduction in the filtering energy loss respectively. Analysis can further be extended for comparison with SPWM scheme with different amplitude and frequency modulation ratio and the other PWM schemes like vector-space

PWM. This is left as a future task. A multi-loop nonlinear compensation strategy has been implemented for the load voltage regulation and the p.f. tracking. The experimental results indicate stable system operation and excellent disturbance rejection.

References

[1]. Mohan.M, Underland.T.M, and Robbins.W.P, 2003. Power electronics: converters, applications, and design. Wiley

[2]. Kundur.P, 1994. Power system stability and control. McGraw-Hil.

[3]. Mete.A.V, and Mehmet.T, 2007. Mathematical modelling and analysis of a unified power flow controller: A comparison of two approaches in power flow studies and effects of UPFC location. *Electrical Power and Energy Systems*, 29(1), 617–629.

[4]. Morsli.S, Tayeb.A, Mouloud.D, and Abdelkader.C, 2012. A robust adaptive fuzzy control of a unified power flow controller. *Turkish Journal of Eleclectrical Engineering and Computer Science*, 20(1)

[5]. Padiyar.K.R, 2007. FACTS controllers in power transmission and distribution, New Age International.

[6]. Baskar.S, Kumarappan.N, and Gnanadass.R, 2010. Switching Level Modelling and Operation of Unified Power Flow Controller. *Asian Power Electronics Journal*, 4(3), 10-19.

[7]. Zhang B.M, and Chen.S.S, 1996. Advanced Power Network Analysis. *Tsinghua Publishing House*, 311-313.

[8]. Haider.A.S, Naz.A, Akhter.F, Azhar.W, and Mehmood.R, 2016. A Novel Efficient Sine Wave Inverter with Custom Programmed PWM and Intelligent Control. *Engineering Technology and Applied Scientific Research*, 6(2), 956-963.

[9]. Noroozian.M, Anguist.L, Ghandhari.M, and Andersson.G, 1997. Use of UPFC for optimal power flow control. *IEEE Transactions on Power Delivery*, 17(4), 1629–1634.

[10]. Qadar.M.R, 2015. Design and simulation of a different innovation controller-based UPFC (unified power flow controller) for the enhancement of power quality. *Energy*, 89(1), 576–592.

[11]. Yahaya.N.Z, Begam.K.M, and Awan.M, 2011. Comparative Assessment of Gate Drive Control Schemes in High Frequency Converter. *Engineering Technology and Applied Scientific Research*, 1(4), 76-83.