Available online www.jsaer.com

Journal of Scientific and Engineering Research, 2014, 1(2):44-54

Research Article

ISSN: 2394-2630
CODEN(USA): JSERBR

Control and Design of High Frequency Power Distribution System

Almond D'Souza

St. Xavier's Catholic College of Engineering, Chunkankadai, Nagercoil

Abstract In this paper, pulse-width-modulated (PWM) resonant inverter with (LCC) topology is presented for high Frequency ac power distribution systems High-frequency AC (HFAC) power distribution system (PDS) has recently received more and more attentions and has abroad application from electric vehicle to Micro-grid. The resonant inverter is commonly used to provide the fixed frequency output for point of load (POL) the inverter system is comprised of simple power and control circuitry. However, the control and implementation of high-frequency resonant inverter is complicated to provide good steady and dynamic performance, because of the worse operating circumstance from parameter uncertainties, inaccuracy model, as well as load and line perturbations The detailed analysis shows that the proposed inverter has very low total harmonic distortion, near-zero switching losses, and fast transient response. Open loop and Closed loop Simulation results are presented to prove the performance of the proposed inverter.

Keywords Harmonic distortion, Resonant converter, Electromagnetic interference, Resonant inverter.

1. Introduction

Present and future high-speed microprocessors are becoming highly dynamic power loads to their power supplies with the simultaneous increase in power demand and decrease in supply voltage level, new challenges arise to the power distribution and power supply design.

High frequency ac (HFAC) power distribution system (PDS) as one of the alternative solutions to powering the future Telecommunication and computer systems Distribution frequency is diverse to different applications and the selection principle mainly depends on the transmission distance. The longer Transmission distance leads to the larger transmission losses.. Generally, a HFAC distribution system uses a front-end inverter as "silver box" to generate high frequency ac voltage for distribution. Then this ac voltage is converted to the specific dc voltage level by a point-of-use ac/dc converter (also known as ac voltage regulator module ac VRM) to power the processors. Compared to the conventional dc PDS, two conversion steps (the rectification in the front-end inverter and the inversion in the VRM) are eliminated in the HFAC PDS. Therefore, HFAC PDS is expected to have higher performance in terms of efficiency, size, cost, and reliability. HF resonant inverter with nearby 25 kHz output is considered as source inverter of auxiliary electrical network, which has to confront more complicated design issues as: (i) lower total harmonic distortion (THD) must be guaranteed to decrease transmission loses, (ii) distributed loads lead to more dynamic load characteristics, (iii) soft switching need be ensured in entire operation scope, (iv) input voltage from battery always varies over a large scope, (v) strong electromagnetic interference (EMI) in EV generates more complicated perturbations

In consideration of these existing issues, possible solutions are studied, such as circuit topology, modulation and control strategy. First, an appropriate resonant topology is critical to provide lower output THD and zero-voltage switching (ZVS) in a large operating scope. Series-Parallel Resonant Topology (SPRT) takes the good characteristics of series and parallel resonant topology while eliminating their drawbacks, such as no-load regulation issue for series resonant topology and high circulating current at light load for parallel resonant topology. The circuit diagram of series-parallel resonant topology (L_s, C_s, C_p) in Fig 1. The resonant circuit has the following Functions:

a) It converts the unidirectional voltage into resonating series current and parallel voltage.

b) It provides ZVS for the inverter switches.

c) It blocks dc component of the unidirectional voltage from Passing to the high-frequency transformer.

In modulation strategy, Pulse Width Modulation (PWM) is used, where the output is controlled by varying the pulse width or duty ratio of the switching waveforms Pulse width modulation or some current controlled switching that reduces the amount of circulating current will improve the partial-load efficiency. The full bridge with PWM is optimal pattern to provide the fixed output frequency, low harmonics and high-power grade.

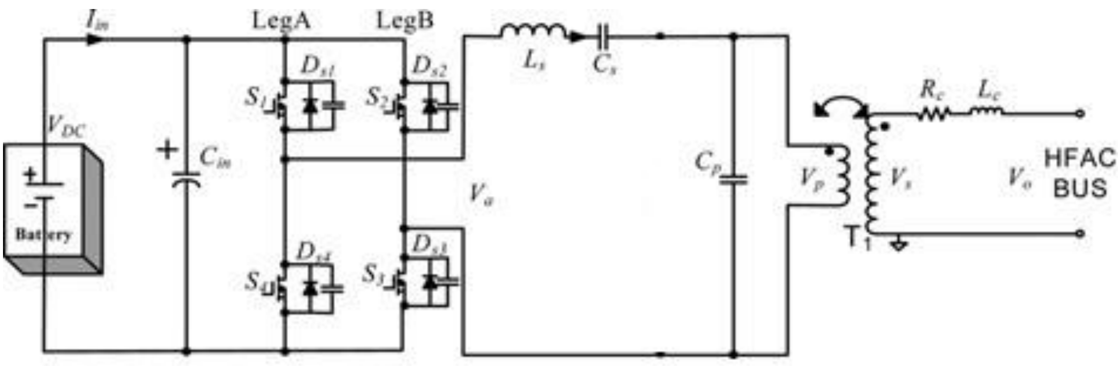

Figure 1: Full bridge resonant inverter

An appropriate controller is significant for dynamic and steady performances. However, the control of resonant inverter is complicated caused by: (i) The strong disturbance from load, input line and components tolerance make it difficult to achieve good control performance and stability. (ii) The inaccuracy from the small-signal model leads to unreliable control ability DSP-based digital control can implement relatively complicated controller however, the operation time grows exponentially along with the increase of controller order. So here PI and PID controller used for controlling the reference voltage to the PWM there by gate pulse may be generated according to the variation of the load and this type of controller are having Good control performance, Fast dynamic response, and Low cost

The proposed system having the following advantages

- Zero switching losses
- Fast transient response
- High efficiency
- Both the power and control circuits are simple

The paper is organised as follows. The mathematical model of LCC resonant inverter is presented in Section 2. The operation of resonant topology and design methodology is presented in Section 3. PI-based controller design is described in Section 4. The simulation and results are demonstrated in Section 5 followed by concluding remarks. The results prove that the proposed controller is having good performance

2. Mathematical model

If the switches in Leg A and Leg B are ideal, the alternative operation produces quasi-square waveform (va) with amplitude Vin and frequency fs. Considering this controllable chopped signal as input of equivalent circuit, the resonant inverter topology can be simplified to Fig. 2, which contains the resonant tank, transformer and equivalent load. The chopped voltage of full-bridge switch (v_a) is connected with series-parallel resonant tank consisting of L_s, C_s and C_p. The resonant tank should exhibit inductive impedance to achieve ZVS of full-bridge switches.

The isolation of input and output sides is a HF transformer, in which the primary voltage is vp and secondary voltage is vs. The secondary side of the transformer is connected with equivalent load through connection impedance formed by R_c and L_c. The nominal load is resistive load (R_L). Load change and non-linear load characteristic are regarded as disturbance represented by additional current source (i_g). The conduction resistance of the switches and the parasitic resistance of the series parallel resonant tank are neglected to simplify the modelling. The traditional state-space-averaged modelling is invalid for resonant converter, because of the violation of small ripple assumption. Sampled-data modelling and phasor-averaging modelling are quite complicated. On account of high-quality factor of resonant parameters to load, a simple modelling based on fundamental component approximation is adopted to design controller. After the harmonics approximation, the mathematic model of resonant converter is derived from kirchoff 's voltage law (KVL) and kirchoff 's current law(KCL), and small-signal linear model is obtained by linearisation of Taylor series expansion. The inductor current and capacitor voltage including v_{cs}, v_{cp}, i_{Ls}, i_{Lp} and i_c are state variables x.
The input variable u is formed by input voltage v_{in} and load current disturbance i_g. The output y is output voltage v_o. Hence, the state equation describing the dynamic behaviour of the resonant inverter is shown below.

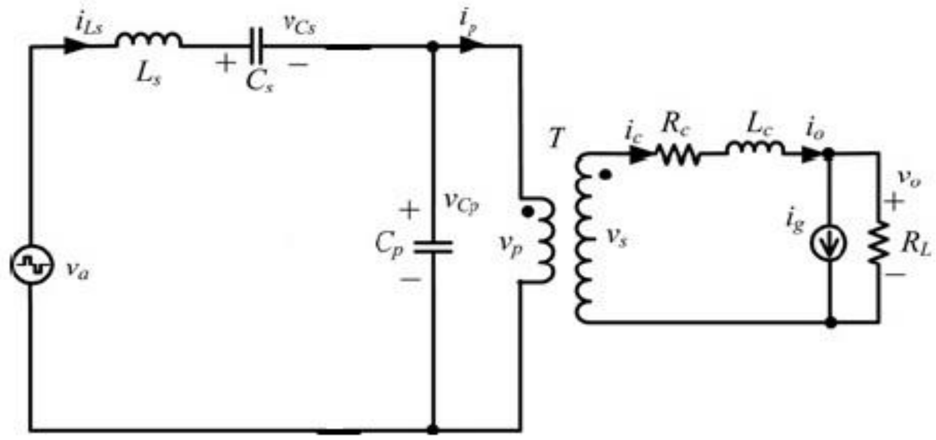

Figure 2: Equivalent circuit of LCC resonant inverter

The parameter vectors are
x=AX + BU
y=CX + DU
$X= [\ V_{cs}\ \ V_{CP} i_{LS} i_C\ ]^T$
$U = [\ V_{in}\ ]^T$
$Y=[\ V_0\ ]$

1. Current through the series capacitor

$$i_{LS} = C_S \frac{dV_{CS}}{dt}$$

2. According to KCL in primary side

$$V_C + V_{CP} + L_S \frac{di_{LS}}{dt} = 0$$

3. KVL in primary side

$$V_C + V_{CP} + L_S \frac{di_{LS}}{dt} = 0$$

4. KVL in secondary side

$$i_C(R_C + R_L) + V_{CP} + i_g R_L + L_c \frac{di_c}{dt} = o$$

From the above equation coefficient of matrix can be written con be as

$$A = \begin{bmatrix} 0 & 0 & \frac{1}{C_s} & 0 \\ 0 & 0 & \frac{1}{C_p} & -\frac{1}{C_p} \\ -\frac{1}{L_s} & -\frac{1}{L_s} & 0 & 0 \\ 0 & \frac{1}{L_c} & 0 & \frac{-R_L + R_c}{L_c} \end{bmatrix}, \; B = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L_s} \\ 0 \end{bmatrix}, \; C = \begin{bmatrix} 0 & 0 & 0 & R_L \end{bmatrix}, \; D = \begin{bmatrix} 0 & -R_L \end{bmatrix}$$

Above A, B, C, D matrix can be used as the model of the system

3. The operation of resonant converter

This series-parallel resonant converter adopts variable frequency control to regulate the output voltage. In Fig 1, diagonal MOSFETs S1 and S4 in full bridge inverter are driven together with 50% duty cycle, whereas the other diagonal MOSFETs S2 and S3 are driven with 50% too, but out of phase. The inverter generates a bidirectional square wave ac voltage to feed into resonant tank. In the secondary side, the current-doubler rectification is used. Current-doubler can be considered as two-phase buck converter. The filter inductor of each phase handles half of output current. The current on secondary transformer winding decreases to half of the output current.

To simplify the analysis of the basic operation of SPRC topology, the following assumptions have been made:

1. The MOSFETs are ideal with no conduction voltage drops, no switching loss and no switching time.
2. The output filter inductor, LF is large enough so that the ripple current is neglected. LF is represented by a current source.
3. The output filter capacitance, Co is large enough so that the output voltage is constant
4. There is no dead-time between the MOSFET on-off state transitions
5. The transformer leakage inductance can be neglected
6. The current through resonant inductor is sinusoidal.

The operation mode of series parallel resonant converter can be categorized by two modes: continuous capacitor voltage mode (CCVM) and discontinuous capacitor voltage mode (DCVM). Their operation principle will be introduced in following sub-sections.

3.1. Operation of Continuous Capacitor Voltage Mode

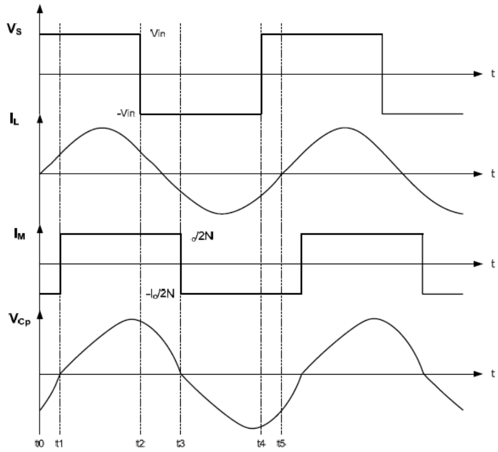

Figure 3: Key operating waveforms of series-parallel resonant converter in CCVM mode

Mode 1 (t0 ~ t1): during this time period, MOSFETs S2 and S3, shown in Figure 1, are off. S1 and S4 are on. At t0, the resonant current is crossing zero. The voltage on parallel capacitor, Cp is at negative value. So is the current of transformer.

Mode 2 (t1 ~ t2): at t1, voltage on Cp crosses to positive side. The current on transformer verses its direction. The resonant current continues to resonant. The voltage source is still positive until at interval t2.

Mode 3 (t2 ~ t3): Q1, Q4 turn off and Q2, Q3 turn on at t2 simultaneously. Since there sonant current lags the applied voltage, Q2 and Q3 turn on at zero voltage switching.

The voltage on Cp in this period stays positive until t3.

Mode 4 (t3 ~ t4): at t3, voltage on Cp reaches zero towards to negative side. The current on transformer thus changes its direction as well. At t4, Q2, Q3 turn off and Q1, Q4 turn on simultaneously. Since the resonant current lags the applied voltage, Q1 and Q4 turn on at zero voltage switching.

Mode 5 (t4 ~ t5): after t4, the negative voltage is applied to resonant tank. Resonant current continues to resonant towards to zero. At t5, the resonant current reaches zero and new cycle starts. During the CCVM mode, the voltage on parallel capacitor although has some distortion on the up slope side, the voltage is continuous without any zero period. This is the case when output load is relatively small. When the output load is increased, the converter will enter DCVM mode where the cap voltage is discontinuous. Its operation will be briefly introduced in following sub-section.

3.2. Operation of Discontinuous Capacitor Voltage Mode

Compare with CCVM mode, voltage on parallel capacitor, Cp in DCVM mode has a short period during which its voltage is clamped to zero voltage. The reason of this is that the resonant inductor current is less than primary transformer current that is reflected from load current at the moment where Cp voltage just reaches zero. There is no current flow into parallel capacitor, Cp. The voltage will remain at zero until the resonant current rises and becomes higher than load reflected current. Then parallel capacitor starts to be charged and voltage rises up. Figure 3 shows the comparison between CCVM and DCVM.

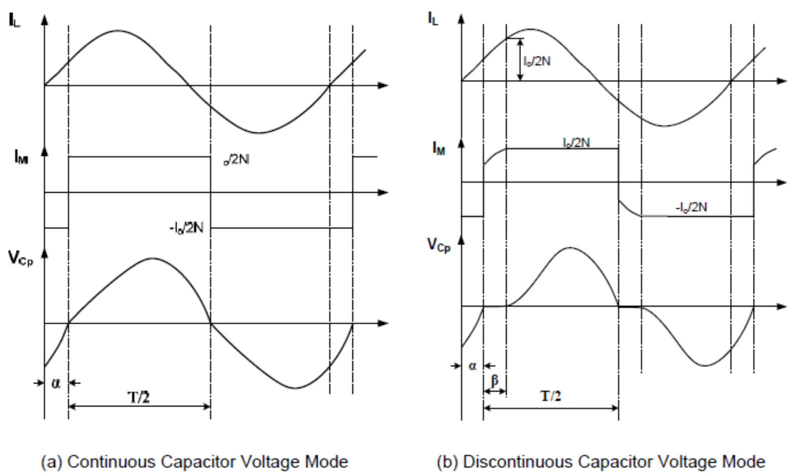

Figure 4: Operation comparison between CCVM and DCVM

During the interval of β in DCVM, the parallel capacitor voltage is clamped to zero. Consequently all the secondary rectifiers conduct and excess load current circulate in the rectifiers. Therefore the DCVM mode operation should be avoided during the design. In next section, the steady state analysis of series-parallel resonant converter will be introduced. The determination of boundary between CCVM and DCVM will be also included.

3.3. Steady-state Analysis of Series-Parallel Resonant Converter

The characteristics of the series-parallel resonant converter will be investigated in this section Conversion Ratio and Operating Frequency Range is analysed. By using complex ac circuit analysis method to analyse SPRC, the dc converter gain can be calculated and given in equation:

$$M = \frac{V_o^{'}}{V_S} = \frac{1}{\sqrt{\left[\frac{\pi^2}{8}\cdot\left(1+k\cdot\left(1-\omega^2\right)\right)\right]^2 + \left[Q_r\cdot\left(\omega-\frac{1}{\omega}\right)\right]^2}} \tag{3.1}$$

Where *Vo* is the output voltage reflected to primary, *VS* is the input voltage, *k* is the capacitor ratio between *Cp* and *Cs*, *k = Cp/Cs*, *Qr = (Ls/Cs)1/2/RL'*, *RL = Vo'2/Po*, *ω = ωs/ωr, ωr* is the angular resonant frequency, *ωr = 2πfr = (Ls/Cs)-1/2*, *ωs* is the angular switching frequency of converter, *ωs = 2πfs* and following equations helps in designing of resonant converter.

Equivalent load resistance:

$$R_{ac} = \frac{\Pi^2}{8} R_L^{'} \tag{3.2}$$

$$R_L^{'} = n^2 R_L$$

Input voltage (V_{rms}) at the link circuit

Voltage across R_a.

$$V_{rms} = \frac{2\sqrt{2}}{\Pi} V_1 \sin\left(\frac{\theta_c}{2}\right) \tag{3.3}$$

$$V_{R_{ac}} = \frac{n\Pi}{2\sqrt{2}} . V_0 \tag{3.4}$$

Output Voltage

$$V_0(n) = \frac{V_0}{V_1} = \frac{8}{n\Pi^2} \frac{V_{Rac}}{V_{rms}} \sin\left(\frac{\theta_c}{2}\right) \tag{3.5}$$

To find L_s, Cs

$$Q_s = \frac{\omega_S L_S}{R_L}$$

$$\omega_S = 2\Pi f_s = \frac{1}{\sqrt{L_S C_S}} \tag{3.6}$$

Figure 5 show the plots of voltage gain as a function of normalized switching frequency for capacitance ratio of 1 and 0.5, respectively. It can be observed that with lower parallel capacitance the converter is running at higher frequency for given dc gain M and Q factor. For example, dc gain M = 1 and Qs = 1, the normalized switching frequency is 1.54 for Cp/Cs = 1 in Figure5 whereas it is 1.6 for Cp/Cs = 0.5, in Figure 6.

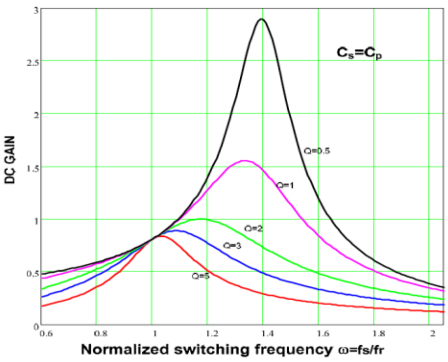

Figure 5: DC characteristic of series-parallel resonant converter, Cp/Cs = 1

When the Q value is further decreased (load is smaller), the difference of normalized switching frequency between two cases will be larger. This indicates that when parallel capacitor is smaller, the characteristic of converter moves towards series resonant converter where the switching frequency range is wider. When parallel capacitor is larger, it provides low impedance, the converter acts more like parallel resonant converter, where the operating frequency range is tighter as load varies.

4. Developement of PI (proportional integrator)-based control

Controllers based on the PI approach are commonly used for DC–DC converter applications. Power converters have relatively low-order dynamics that can be well controlled by the PI method. The system is simulated with a switching frequency of 50 KHz. The simulated converter output voltage Vo and load current Io for applied at 10 ms. It is observed that the PI controller for the LCL configuration regulates the output voltage

Proportional Constant (Kp) = 0.05

Integral Time Constant (Ki) = 25

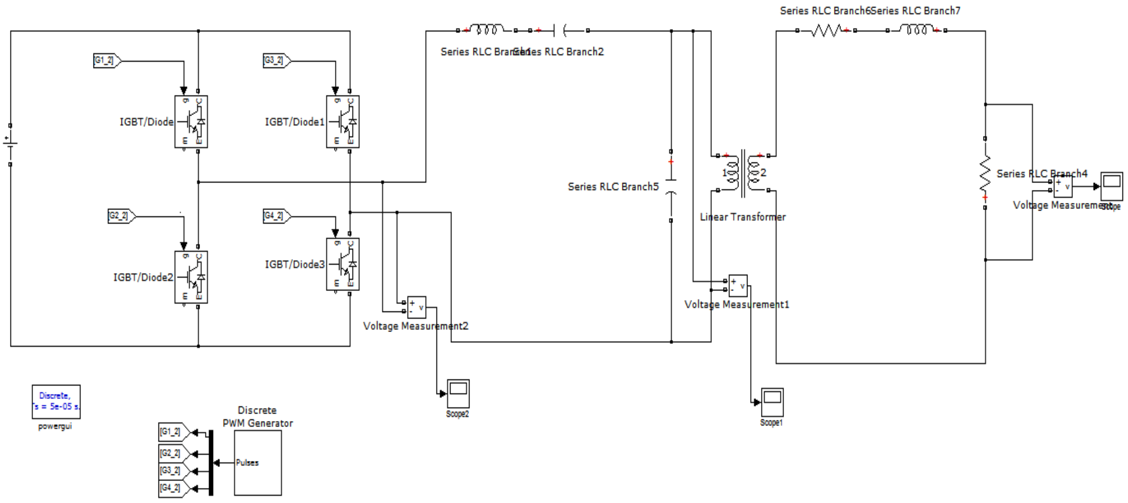

Figure 6: Open Loop Simulation

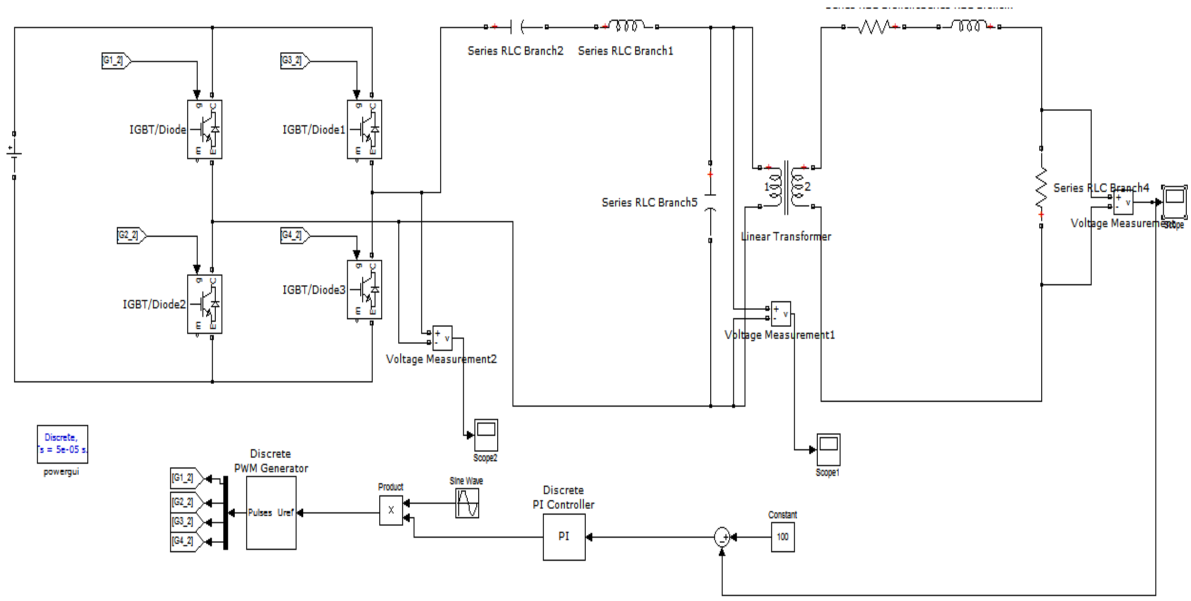

Figure 7: Closed Loop Simulation

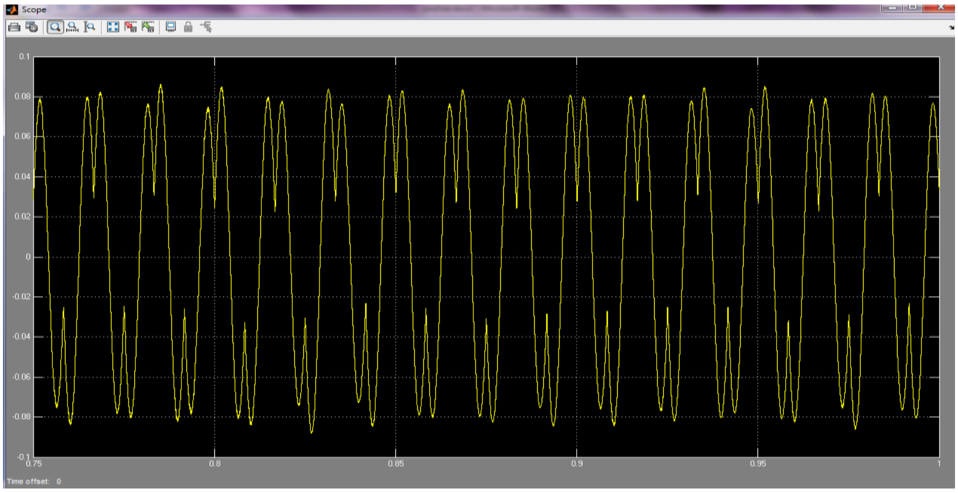

Figure 8: Output of Open Loop Simulation

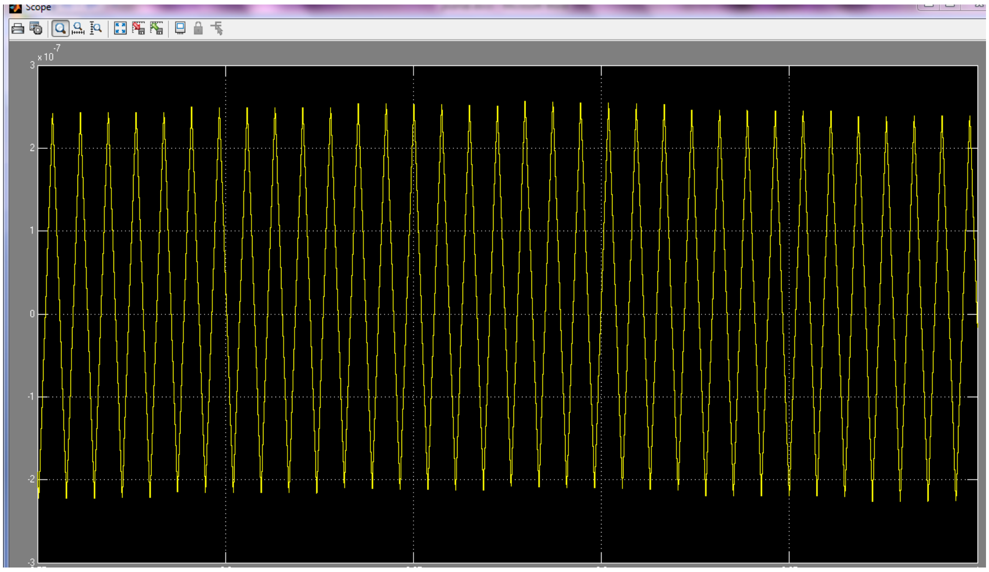

Figure 9: Output of Closed Loop Simulation

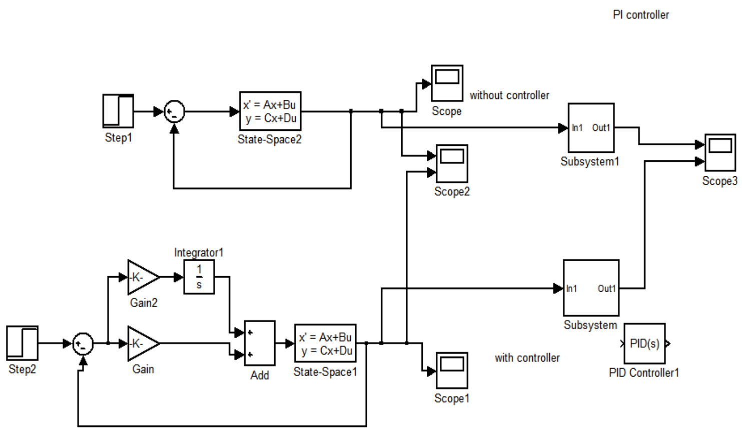

Figure 10: Comparison between with and without controller

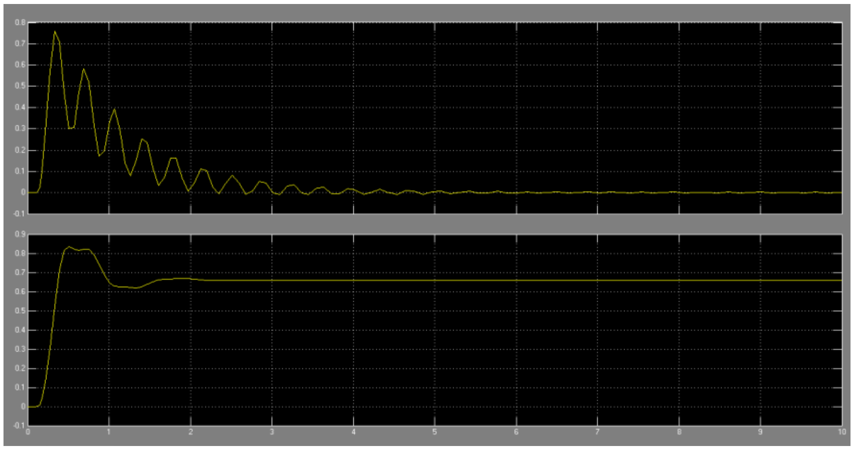

Figure 11: Comparison between output

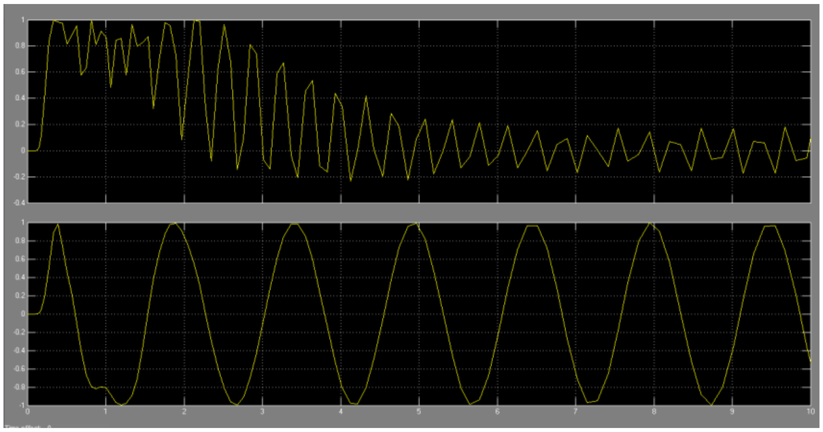

Figure 12: Comparison of output voltage between characteristics in respect to with and without controller with and without controller

5. Simulation results

The simulation results show that the proposed inverter generates near sinusoidal voltage waveform at the output. Simulation results also show that ZVS is not lost at light load for the whole input voltage range. The simulation diagram of the open loop system and its output of voltage waveforms are shown in Figures 8 and 9. The closed loop circuit model is shown in Figure 9 the output is sensed and it is compared with the reference voltage. The error is given to a PI controller; the output of PI controller adjusts the pulse width to bring the voltage to the set value. Figure 9 shows the closed loop inverter output of voltage waveform. The mathematical model of resonant inverter is taken in the figure 11 is compared with presence and without presence of the controller there by its output characteristics is analysed .The control loop uses the modulated integral control as a feed forward loop to provide pre-regulation for the feedback loop. A load voltage feedback loop is also included to compensate the resonant tanks of the inverter. Simulation results show that the proposed inverter has fast transient response against the load variations.

6. Conclusion

HFAC PDS implemented as power source is examined in this paper. The simulation results are in line with the predictions. This work deals with simulation studies .Hardware is not in the scope of this work. The simulation results are proved that the proposed topology has advantages like low switching losses and reduced stress. Also it providing near sinusoidal output voltage (THD less than 2% at the rated load). This sinusoidal voltage is used for induction heating .This system operates at high efficiency due to soft switching. Both the power and control circuits are simple, and have only two active switches. This topology is, therefore, an attractive candidate for the front-end inverter in HFAC distribution systems to power the future telecommunication andComputer system.

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