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Low Power Strain and Dimension Aware SRAM Cell Design Using a New Tunnel FET and Domino Independent Logic

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Abstract: Mechanical strain and dimension in silicon leads to band splitting and alters the effective mass which results in carrier mobility changes. Induced strain and dimension effects on channel can be either "tensile" or "compressive". NMOS and PMOS devices have different desired strain and dimension types in the longitudinal, lateral and Si-depth dimensions. The small band gap tensile strained silicon is more compatible than conventional silicon processing for low power circuit design. In this paper, we propose strain and dimension aware circuit (SDAC) design using new physics model and domino clock and input dependent (d-INDEP) logic. In SDAC design, an optimal depleted strained TFET physics model is used to improve the on-current and steep sub-threshold swing, which are main cause of strain and dimension effects. The performance of any logic design is reduced by increasing leakage current and variability of parameters, which affects the power consumption problem. The problem is overcome by the d-INDEP logic that reduces leakage current as well as affected power without extra logics. The proposed physics and low power logic is tested with SRAM cell and simulated in HSPICE tool. The simulation result shows the effectiveness of proposed SDAC design in terms of power and delay.

Keywords: Strain, Dimension, d-INDEP, Optimal depleted strained TFET, SRAM, HSPICE.

1. Introduction

Tunnel field effect transistors (TFETs) have better sub-threshold swing and low leakage current than CMOS design and it is reasonable for future sub-micron applications [1, 2]. From a conventional MOSFET, the current transfer and saturation characteristics of TFET are very unique and in complex circuit design the high leakage currents and short channel impacts create tougher. Numerous novel device modeling have proposed in order to tackling this issue [3, 4].

The role of (strain and indium) alloy composition on the device performance of Ge homo-junction by a significant strain dependent enhancement in ION current for both n- and p-type Ge TFETs [5-7]. The new materials are accomplished by high tunneling current and with lower band gap. Another unsolvable issue of TFET is scaling (also called dimension problem), which increment the static and dynamic power consumption; out of this static power turns out to be too high [8 - 11]. From the characteristics of output, furnish some interesting insights about TFET with the dimension impacts on both up and down scaling [12]. Not at all like MOSFETs, the asymmetric current conduction as TFET conduction currents show only in the reverse-bias region. In this way, in circuit design it is must to overcome the strain and dimension impacts, to employ TFET for low power applications.

Our contributions

The strain and dimension impacts are investigated and propose stain and dimension aware circuit (SDAC) design utilizing optimal depleted strained TFET physics model and the d-INDEP low power logic. Know to my best of knowledge, there have been very few studies of the effect of strain and dimension on the performance of TFET. The main

goal of proposed SDAC design is to compromise those feelings and make effective awareness against strain and dimension impacts in TFET.

The remainder of this paper is sorted as follows. The current works related to our contribution is reviewed in Section 2. The problem methodology and system model of proposed solution is given in Section 3 and the detailed explanations are briefly discussed in Section 4. Section 5 elaborates the simulation result and performance analysis. Finally, the paper finishes up in Section 6.

2. Related works

Lunog et al. [13] have presented a strained Si (sSi) nanowires array of n-TFETs with gates all around (GAA) yielding ON-currents with a presented supply voltage. The main drawback of the technique is the logic gate does not depend on which gate is placed next to it. Kim et al. [14] have proposed a combination of TFETs with asymmetrically doped p+-i-n+ silicon nanowires (SiNW) channels on a bendable substrate. The NOR logic operation is non-sustainable for up to 1,000 bending cycles with wide transition width of ~0.26 V is the main drawback. Lahgere et al. [15] have proposed a TFET based on charge plasma (CP) and negative capacitance (NC) for enhanced ON-current and steep sub threshold swing. The dopingless silicon nanowire used with CP has a genuine advantage in the process of both technology boosters and it enables the low thermal budget, process variation immunity, and excellent electrical characteristics in contrast with counterpart doping-less (DL) TFET (DL-TFET). Bi et al. [16] have introduced a library of TFET-based current mode logic components, (TEFT CML) which cover all basic logic gates. However, the regular layout of SRAM arrays makes them a good candidate to achieve long uncut fins that maximize the effects of stress in TFET CML. A physics model for double-gate TFET using the effect of Ferro-electric (Fe) gate oxide on hetero-junction and band-gap engineering based electro-statically doped source/drain (EDSD) is introduced by Singh et al. [17]. The comparison of various low band gap source region materials very low on-off current ratio was the drawback. Kumar et al. [18] have enhanced the performance of impact ionization SOI FETs by utilizing strained channel and doping-less concept. Very low carrier mobility was the drawback. The impact of monolayer transition metal dichal cogenides (TMDC) materials and monolayer TMDC alloys on the performance of thin tunneling field-effect transistors or thin-TFETs are explored by Datta et al. [19]. However, the design has to take care of mismatch and must ensure both read stability and write ability, still presenting good speed and power metrics.

3. Problem methodology and system model

3.1 Problem methodology

Liu et al. [20] have present a tensile-strained Ge/InGaAs TFET-based SRAM circuit utilizing a few access schemes and research the cell access design impact on static and dynamic performance. SRAM cells utilizing outward access transistors exhibit wide read and write static noise margins, yet suffer from increased read delay times. To resolve the degraded read delay time 7T SRAM cell architecture is utilized. The tunable tensile-strained Ge/InGaAs hetero-junction TFETs used to explored the performance impact of strain state on SRAM operation. This model provides successful read and write capability, however the read delay time is very high. The SRAM cell standby power is unequivocally relies upon both operational voltage and the Ge strain level. At the point when contrasted with CMOS-based SRAM designs under ultralow voltage operation, the strain modulation between 1.5% and 3% revealed considerable (mostly similar) diminishment in cell standby energy. Generally, the down scaling of lower order dimension affects the OFF-state leakage current and increases exponentially due to the non scalability of threshold voltage since the sub threshold swing. Another major insurmountable limit of tensile-strained Ge/InGaAs TFET is strain effect which dictates that the switching slope of the transistor cannot go extremely beneath and without drastically expanding the static power consumption, it is impossible to scale down the supply voltage.

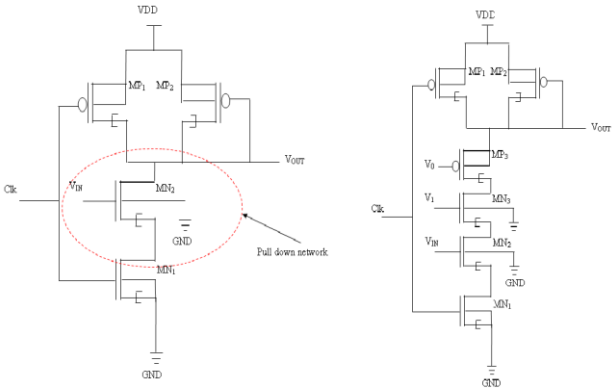
To conquer these issue the proposed strain and dimension aware circuit (SDAC) design with the help of proposed optimal depleted strained TFET and domino independent (d-INDEP) logic is utilized. The high on-current accomplished by this optimal depleted strained TFET structure, and the average sub threshold swing successfully diminished. The effect of strain and dimension impacts controlled by the threshold voltage with the design parameters, for example, strained Si layer thickness and gate length. The new TFETs possess potential to overcome thermionic emission limit and therefore allow for low supply voltage operation. In today scenarios, because of dimension impacts the low power circuit design is not guaranteed. This issue is overwhelmed by domino clock and input dependent (d-INDEP)

logic design, which reduces leakage current with least delay. In this way, it is exceptionally appropriate to design SRAM cell with limited read delay time and low power consumption. The proposed design is tested with the SRAM cell and performance is contrasted with the tensile-strained Ge/InGaAs TFET-based SRAM [20] in terms of power and delay.

3.2 System model of proposed strain and dimension aware circuit (SDAC) design

In SDAC, an optimal depleted TFET consolidates a low band-gap source injector and inherent high drive current with hypothesize to excellent electrostatic control of steep turn on characteristics. This TFET transistor in conjunction with a low band gap source material would enable a higher inter-band tunneling rate, in a configuration. To make the full outline, the source material Ge has roughly 50% of band gap and littler effective mass. The outline include an overlap with the gate would potentially instigate higher tunneling rate because of vertical tunneling within the Ge source. The lateral tunneling is restricted by the thickness of inversion layer of the source channel junction in the "ON" state of the transistor, and which is constrained by the junction's cross section.

For implementing high speed logic designs, domino logic is the most effective circuit configurations. The advantages offered by domino circuits are faster transitions and glitch-free operation. The development of the dynamic logic methods depend on either PMOS or NMOS transistors and it runs 1.5-2 times quicker than static CMOS logic since dynamic gates present much lower input capacitance for the same output current and a lower switching threshold. The keeper transistor in domino logic has to solve the charge leakage problem with the higher transitions states of output node and it give the low resistive way between the pull down network and the power supply. The inverter using domino logic is appeared in Fig. 1 (a). Initially the domino logic circuit is in pre charge phase, when the clock signal is low. At this phase, the output is charged to VDD through MP_1 transistor. The keeper transistor will turn 'ON', when the V_{OUT} of the circuit is low. When the clock signal is high, the circuit goes into the evaluation phase and the output is discharged to ground, according to the input combination of pull down network. Amid the evaluation phase (from 0 to 1) the inverter output voltage can also make one transition. At the cost of delay, the keeper transistor



(a) (b)

Figure.1 Inverter design: (a) using domino logic and (b) using d-INDEP logic

(MP_2) enhances robustness and power dissipation and small sized keeper is desired for fast application.

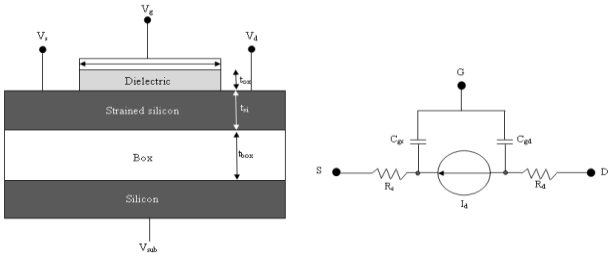
Fig. 1 (b) illustrates the proposed domino with clock and input dependent (d-INDEP) transistors logic inverter. In this design, the MP_3 and MN_3 are the two transistors; V_0 and V_1 is the gate terminal of these transistors which is clock and input logic dependent respectively. The body terminal of all PMOS and NMOS transistors are associated to VDD and GND individually. When clock signal is low, then V_{OUT} should be low so that MP_1 and MP_3 transistors is turn on and the logic circuit d-INDEP comes in pre charge phase. In which output node is charged to VDD through $MP_1$and MP_3 transistors. Then, the keeper transistor (MP_2) will turn on when V_{OUT} of the circuit is low. When the clock signal is high, the circuit enters into the evaluation phase and when the input voltage V_{IN} is high then output should be high, so that the dynamic node becomes low. When the input V_{IN} is low then output node should be low, so that dynamic node becomes high.

4. Proposed strain and dimension aware circuit (SDAC) design

In this section, the detailed portrayal of an optimal depleted strained TFET physics model and the low power ensured d-INDEP logic is displayed.

4.1 Optimal depleted strained TFET physics model

A MOS gate is utilized by TFETs to control the band-to-band tunneling across a degenerate p-n junction. The schematic diagram of an optimal depleted strained TFET is appeared in Fig. 3. Regularly the device is off, when zero bias is applied to the gate, the conduction band minimum of the channel is over the valence band maximum of



(a) (b)

Figure.2 Optimal depleted strained TFET: (a) cross section and (b) equivalent circuit

the source, and thus band-to-band tunneling is suppressed. A tunneling window opens up as the conduction band of the channel is moved beneath the source valence band. In this tunneling window tunnel the electrons in the valence band with energy is to empty states in the channel and the transistor becoming ON. The operation principle is same for the p-channel TFET with source channel and drain conductivity types switched. The device comprises of a high-k dielectric layer with a thickness of t_{ox}, a strained Si layer with a thickness of t_{si}, t_{box} as a thickness of a buried oxide layer, and a gate with a length L.

In Fig. 2 (a), the model can operate both *n* and *p* channel modes. The V_s represents source voltage, V_d represents drain voltage, V_g represents gate voltage and V_{ref} represents maximum reference voltage. To align the valence band and channel conduction band, the V_{ref} is required. In n-channel mode the tunneling occurs in the source side, while in p-channel mode tunneling occurs in the drain side. An electron inversion layer is created in the channel at the interface with the gate dielectric when a gate voltage greater V_{ref} is applied. From the source valence band to conduction band the tunneling takes place in the inversion layer of the channel. The drain side low-K gate oxide and the tunneling junction high-K oxide are used to reduce the ambipolar current at the drain side. Thus, the low-K gate oxide is utilized.

Fig. 2 (b) represents the equivalent circuit of optimal depleted strained TFET, which contains a voltage controlled current source to model the drain current, capacitors and source and drain series resistors.

4.1.1. Drain current (I_d) model

The asymmetric source/drain junction brings about asymmetric characteristics both as a function of drain-source bias V_{ds} and gate-source bias V_{gs}. The $V_{ds} < 0$ with positive V_{gs} in the negative drain-source bias polarity, toward a current maxima band-to-band tunneling current increases first, trailed by an exponentially-increasing diffusion current. The tunnel junction can move from the source-channel junction to the drain-channel junction, when there is negative gate-bias, with positive drain-source bias. The total drain current T_{I_d} as follows,

$$T_{I_d} = \left(\frac{W\,TCH\,q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m_e^*}{E_g}}\, f\, E V_{tw} e^{\frac{-4\sqrt{2m_h^*}\,E_g\,E}{3q\hbar}} \right) + \left(S + I_1\left|-V_{gs}, V_{ds}\right|\right) - \left(W\,TCH\left(\frac{V_{tw}}{V_{gs}+TCH} E\, e^{1+\frac{V_{tw}+V_t}{2V_{gs}}} + V_{tw}\left(e^{\frac{V_{gs}}{V_t}-1} \right) \right) \right) \quad (1)$$

where the first terms represents the drain to source tunnel current also denotes as I_1 with the bias dependent tunneling window V_{tw} and a dimensionless factor f, which accounts for the super linear current onset in the output characteristic, m_e* and m_h* is the energy and hole effective masses, E_g is the semiconductor band gap, and $\hbar$ is the reduced Planck's constant. The second term is ambipolar current and it added to the model by copying the current for $V_{gs} > 0$ to $V_{gs} < 0$ and multiplying the current by a scaling factor (*S*). The third term defines the diode current.

4.1.2. Capacitance model

The gate to source capacitance (C_{gs}) is very smaller than the gate to drain capacitance (C_{gd}) in TFET functioning model in the arrangement of optimal depletion. The scaling function of C_{gs} is dependence on the fringe capacitance between know or defined scaling geometries. The C_{gs} is modeled as,

$$C_{gs} = CGS0 \cdot W \quad (2)$$

Where, the coordination between the gate to source region at the time of maximum V_g is represented by *CGS0* and *W* is the width of TFET transistor. The C_{gd} is modeled as accompanies:

$$C_{gd} = 0.31C_i + (0.9C_i - 0.31C_i)\frac{0.0001}{2C_i}\sqrt{\Delta^2 + \left|\frac{C_i}{0.0002V_{gs}}\right|^2} \quad (3)$$

The intrinsic gate oxide capacitance (C_i) is modeled as,

$$C_i = \frac{LW\,\varepsilon_O\,E_{OX}}{t_{ox}} \quad (4)$$

4.1.3. Surface potential model

The depletion charge is considered in the sub threshold region and the Poisson equation can be written as,

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi(r,x)}{\partial r}\right)+\frac{\partial^2\phi(r,x)}{\partial x^2}=\frac{q\,N_i}{\varepsilon_{si}} \tag{5}$$

where the two-dimensional potential is $\phi(r, x)$, in the partition regions Ni are the diverse doping densities, and ε_{si} represents silicon dielectric constant. The '*r'* differs from zero to R ($0 \le r \le R$), and x fluctuates from the source to the drain. Since in the radius direction the potential is parabolic and it can be comprehended utilizing the 2D polynomial approximation

$$\phi(r,x)=\phi_C(x)+\frac{2C_{ox}\,R_S\left(V_{gs}-V_{fb}-\phi_S(x)\cdot R_d\right)}{\varepsilon_{si}} \tag{6}$$

Here, $\phi_c(x)$ is the center and $\phi_s(x)$ is the surface potentials in channel direction, respectively. The surface potential in the channel direction is approximate by the inter-band tunneling probability and it is assumed as a modified Poisson equation, generating a characteristic length scale λ for the surface potential variation.

$$\frac{\partial^2\phi_S(x)}{\partial x^2}+\frac{\phi_S(x)}{\lambda^2}=\frac{q\,N_i}{\varepsilon_{si}}-\frac{V_{gs}-V_t}{\lambda^2} \tag{7}$$

With an optimal depleted condition, the first region is present in the region of $-L_1 \le x < 0$ and the equivalent gate oxide thickness is $t'_{ox} = \Pi^{t_{ox}}/_2$for the gate fringing field as accompanies:

$$\phi_{S_{optimal}}(x)=X\,e^{\frac{x}{\lambda_1}}+Y\,e^{\frac{-x}{\lambda_1}}-\lambda_1^2\frac{q\,N_i}{\varepsilon_{si}}-\frac{V_{gs}-V_t}{\lambda_1^2} \tag{8}$$

where $\lambda_1 = \sqrt{\frac{\varepsilon_{si}R^2\ln(1+\pi^{t_{ox}/_2})}{2\varepsilon_{si}}}$

The surface potential solution in optimal depleted region is asserted as,

$$\phi_{S_{optimal}}(x)=X\,Y\left(x+L_{optimal}\right)^2-2V_{gs} \tag{10}$$

Where $L_{optimal}$ is the length of optimal depletion region. Similarly, the second region surface potential is expressed as,

$$\phi_{S2}(x)=\left(V_{gs}-V_{fb}\right)- \left(V_{gs}-V_{fb}-2V_{gs}-\phi_S(x)\right)n\cosh\left(\frac{q\,N_i-L_2}{\varepsilon_{si}}\right) \tag{11}$$

In Eq. (11) the length L_2 is unknown. Then, utilizing the following boundary conditions between region optimal depletion and second, the values of $L_{optimal}$ and L_2 are find and given underneath;

$$L_{optimal}=\sqrt{\frac{2\,\varepsilon_{si}\,\phi_S(0)+V_t}{q\,N_{si}}} \tag{12}$$

$$L_2=\lambda_2\cosh^{-1}\left(-\frac{V_{gs}-V_{fb}}{V_{gs}-V_{fb}-2V_{gs}-\phi_S(x)}\right) \tag{13}$$

where $\phi_S(0)$ stands for the surface potential at position $x = 0$ as follows:

$$\phi_S(0)=-\left(V_{gs}-V_{fb}-2V_{gs}-\phi_S(x)\right)^2+ 2\left(V_{gs}-V_{fb}\right)\frac{q\,N_i\,\lambda^2}{\varepsilon_{si}}+ 2V_{gs}\,\zeta^2+\left(V_{gs}-V_{fb}-\frac{q\,N_i\,\lambda^2}{\varepsilon_{si}}\right) \tag{14}$$

4.1.4. Threshold voltage model

The sub-threshold swing is a function of channel length and the interface trapped-charge density is designed as,

$$S_{th}=1+E_C\frac{C_d}{C_{cox}}+C_{cd}+\frac{\left((C_{dsc}+C_{dscd}\,V_{ds}+C_{dscb}\,V_{bs})e^{-c_1\frac{L_{eff}}{2L_t}}+2e^{-c_1\frac{L_{eff}}{L_t}}\right)}{C_{ox}} \tag{15}$$

where C_d is the depletion capacitance, C_{dsc}, C_{dscd}, and C_{dscb} is the channel coupling capacitance. C_{cd} is the capacitance due to interface trapped-charge density and the parameter E_c utilized to remunerate the errors in the depletion width capacitance. L_{eff} represents the effective-channel length and C_1 is the first coefficient of short channel impacts on

threshold voltage. The threshold voltage of this model represents as follows:

$$V_{TH} = V_{th_i} + \delta \left(\begin{array}{l} K_1 \sqrt{1 + 2\phi_f + \phi_s + \frac{N_L}{L_{eff}}} - V_{bs} - \\ K_2 V_{bs} + \left(K_3 + K_{3b}\, V_{bs}\right) \frac{T_{ox}}{W_{eff} + W_0} 2\varphi_f \\ - 4 S_{th} V_{ds} \left(\frac{V_{bi} - 2\phi_f}{V_{ds}} - \left(E_1 + E_2\right) V_{bs} \right) \end{array} \right) \quad (16)$$

where K_1 and K_2 are the first order and second order body effect coefficients, K_3 is the narrow width, K_{3b} is the body effect coefficient, W_0 is the narrow width parameter, T_{ox} is the gate oxide thickness, L_{eff} is the effective-channel length, W_{eff} is the effective width of the device, and V_{th} is the threshold voltage for long channel TFET at V_{ds} = 50 mV and V_{bs} = 0 V. In TFET the value of δ is +1 for n-channel and −1 for p-channel. This model assumes that the mobility is independent of V_{ds} and hence the lateral electric field. The unified formulation of effective mobility defined as follows:

$$\mu_{eff} = \frac{\mu_1}{1 + \left[\mu_2 \left(\frac{V_{gs} + V_{th}}{t_{ox}} \right) + \mu_3 \left(\frac{V_{gs} + V_{th}}{t_{ox}} \right)^2 \right] \left(1 + \mu_4 V_{bs}\right)} \quad (17)$$

Where, the low-field mobility is μ_1, μ_2 and $\mu_3$is the first and second order mobility degradation coefficients, respectively and μ_4 is mobility degradation coefficient due to the body-effect.

The depletion width becomes non-uniform along channel in a long channel TFET especially when the drain bias is high. This phenomenon, additionally named as bulk charge effect, causes V_{th} to differ along the channel. The bulk effect A_b is given as takes after:

$$A_b = \left\{1 + A_{b1}\left[x_1 A_{b2} - x_2 A_{b3} + A_{b4}\right]\right\} \frac{1}{1 + K_{ETA} V_{bs}} \quad (18)$$

Where $A_{b1} = K_1 / (2\sqrt{(2\phi_f - V_{bs})})$, $A_{b2} = 1$,
$A_{b3} = A_{gs} (V_{gs} - V_{th}) (L_{eff} / (L_{eff} + 2\sqrt{J_{dep}}))^2$,
$x_1 = x_2 = (A_0 L_{eff}) / (L_{eff} + 2\sqrt{J_{dep}})$, and
$A_{b4} = B_0 / (W_{eff} + B_1)$

where A_0 is the bulk charge effect coefficient for channel length, B_0, B_1 is the bulk charge effect coefficient for channel width, and it offset

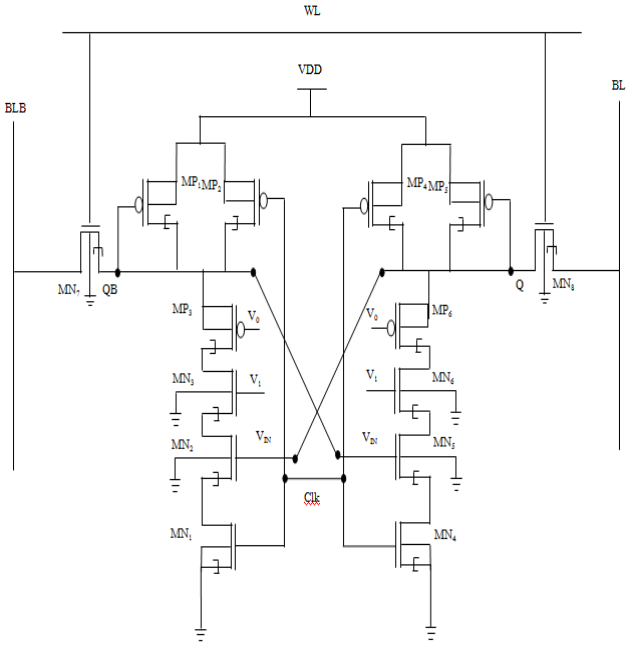


Figure.3 SRAM cell with d-INDEP logic

respectively, J_{dep} is source/drain junction depletion thickness in channel region, A_{gs} is the gate bias coefficient and K_{ETA} is the body-bias coefficient of bulk charge effect.

4.2 SRAM cell using d-INDEP logic

The SRAM cell with d-INDEP logic is delineated in Fig 3. Before the write operation, between the two inverters the feedback connection is cutting off. Through an additional NMOS transistor N7 the feedback connection and disconnection are performed. The cell just relies upon (bit line bar) BLB to perform a write operation. The write operation starts by turning N7 off to cut off the feedback connection. The SRAM cell resembles like two cascaded inverters. BLB transfers the complement of input data to QB this energies to create Q, which assistant drives and changes Q. In each (previously and after) read/write operation both (bit line) BL and BLB are pre-charged "high". When writing "Low", BLB is kept "High" with negligible write power consumption. The write "High", BLB is discharged to "Low" with comparable power consumption to a conventional write. Amid write operation, the write circuit will not discharge one of the bit lines and the activity factor of discharging BLB is less than "High". During read operation, the cell behaves like a conventional SRAM cell and N7 is kept on.

The BL and word line (WL) are utilized while writing into the cell, where read line (RL) isn't used. While reading BL and RL are utilized, where word line (WL) isn't utilized. Hence only one bit line

usage diminishes the power required to charge and discharge the bit lines to approximately half. The power consumption from charging the bit line diminishes by approximately a factor of 2 because in read operation only one bit line is charged instead of two. The bit line is charged during a write operation about half of the time instead of every time when a write operation is required, here equal probability of writing 'Low' and 'High' has been accepted. While writing, the data need to be written will be loaded on BL and WL will be actuated. Strong access transistor N_8 permits bit line to overpower the cell, so that required data will be written into the cell. To write '1' into the cell, the BL is charged to VDD.

On the off chance that the data need to be written is '0', then BL should be at logic low, and WL is pulled to VDD. To read data from the cell, initially BL is being pre-charged to VDD. After pre-charging the bit line RL is actuated. Contingent on whether the BL discharges or holds the held charge, data stored in the SRAM cell can be chosen. If BL discharges after pulling the RL to VDD, it indicates SRAM cell is storing 'Low' in it. If bit line holds the held charge then the data stored is 'High'. Hence WL is inactive in read mode.

5. Simulation results

The performance of proposed SDAC design is deeply examined with the presumption of channel width of NMOS transistor was twice of the respective PMOS channel length; it was sized to triples of the respective pull-down NMOS. With different supply voltages the CAD simulations were carried out through HSPICE tool. Fig. 8 demonstrates the voltage transfer characteristics of proposed LPAEFF design taken from HSPICE tool by differing supply voltages from 1*V* to 1.4 *V*. The cell ratio is changed to make the variety in the speed of SRAM cell. The size of the driver transistor increases when the cell ratio increases, hence current also increases. As increase in current, the speed of the SRAM cell also increases and in this manner changing the cell ratio we got corresponding signal to noise margin (SNM). The channel doping concentration is 10^{17} cm^{-3}, the thickness of silicon is 10nm, and thickness of oxide is 50nm. The source and drain doping concentration is 10^{20} cm^{-3} and 5×10^{18} cm^{-3} respectively.

5.1 Impact of SNM in read and write operation

Data retention of the SRAM cell, both in standby mode and in advanced technology nodes amid a read access, is an important functional constraint. The cell becomes less stable with expanding leakage currents in lower supply voltage and increasing variability, all resulting from technology scaling. Generally the SNM characterizes stability as the maximum value of DC noise voltage that can be endured by the SRAM cell without changing the stored bit. With the cross-coupled inverters, the two DC noise voltage sources are placed in series. The minimum value of noise voltage which is necessary to flip the state of the cell is recorded as Read SNM (RSNM). The voltage transfer characteristic of one cell inverter is inverses of the other cell inverter. The resulting two-lobed graph is called a "butterfly" curve and is used to determine the SNM. Its value is defined as the side length of the largest square that can be fitted inside the lobes of the "butterfly" curve. More the SNM value, higher is the read stability of SRAM cell.

Write SNM (WSNM) is the measure of ability to write data into the SRAM cell. Its voltage is the maximum noise voltage present at bit lines amid successful write operation. When noise voltages exceeds the write margin voltage, then write failure occurs. In this section, a static approach is introduced for measuring write margin. The cell is set in the write operation while writing a 'High' into the cell. WSNM is estimated utilizing butterfly curves as appeared in Fig. 4, which is gotten from a dc simulation sweeping the input of the inverters. Only one cross point should be found on the butterfly curves, for a successful write, demonstrating that the cell is mono-stable. WSNM for writing 'High' is the width of the smallest square that can be embedded between the lower-right half of the curves. The final WSNM for the cell is the minimum of the margin for writing 'Low' and writing 'High'.

The performance correlation of proposed SRAM cell is contrasted with distinctive SRAM cells, for example, outward, CMOS, hybrid and inward [20] with the operating frequency of 0.3 and 0.6 *V* in terms of RSNM and WSNM. The result esteems are plotted in Fig. 5, and it is unmistakably depicts the RSNM of proposed SRAM-SDAC is varying very gradually with respect to varying width of transistors ratios and it is very efficient than existing SRAM for both 0.3 *V*.

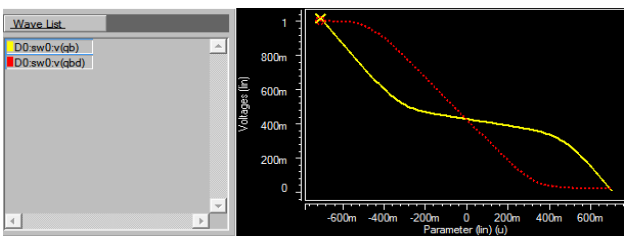
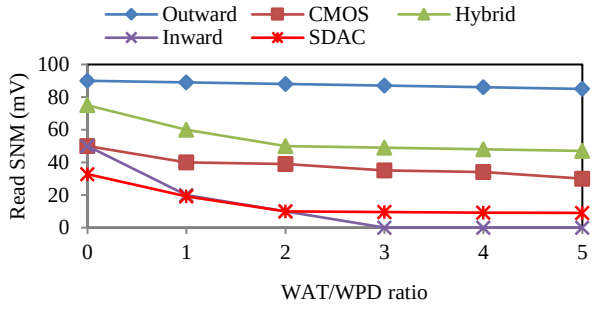
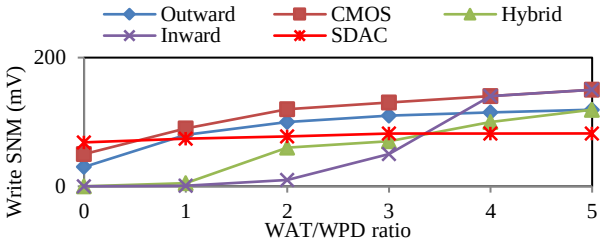


Figure.4 Screenshot of SRAM butterfly curve taken from DC analysis

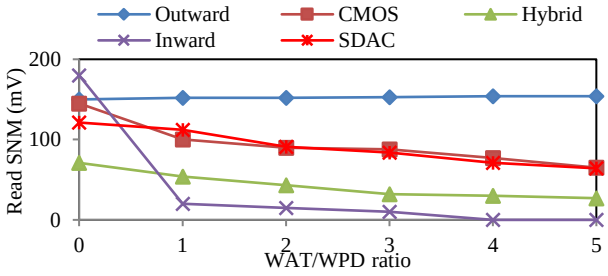


(a)

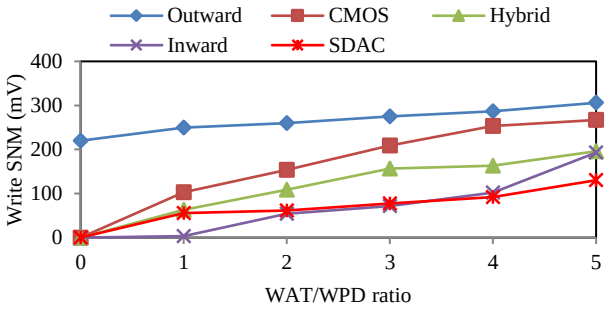


(b)

Figure.5 SNM of: (a) read and (b) write operation with 0.3 V



(a)



(b)

Figure.6 SNM of: (a) read and (b) write operation with 0.6 V

The result values are plotted in Fig. 6, and it is clearly depicts the RSNM of proposed SRAM-SDAC is varying very gradually with respect to changing width of transistors ratios and for both 0.6 *V* it is very efficient than existing SRAM. For area analysis, compared to existing circuit, the proposed circuit consumes extra transmitter but not too-much. However, the proposed circuit owned physics model is strain and dimension aware design.

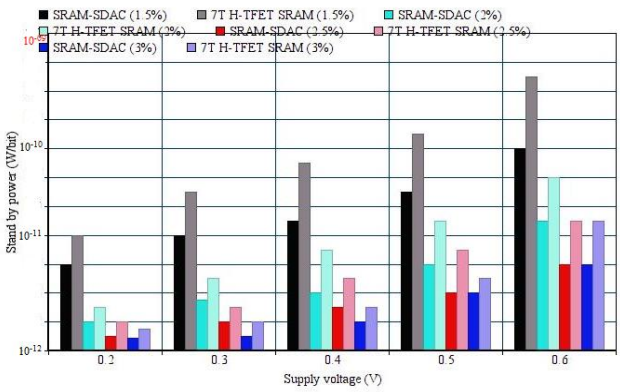


Figure.7 Standby power comparison with varying supply voltage

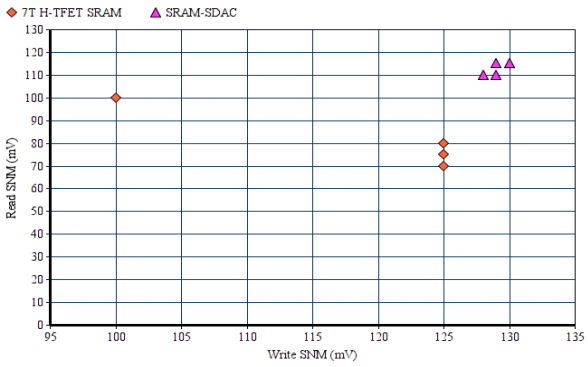


Figure.8 Read SNM with write SNM

Fig. 7 compares the SRAM cell standby power as a function of supply voltage. The standby power was found to reduce for decreasing operational voltages, as expected. Moreover, at every supply voltage between 0.2-0.6 *V*, the standby power of the proposed SRAM-SDAC design is very less compare to the existing 7T H-TFET SRAM cell. Although higher strain H-TFETs provide some performance improvement, the proposed physics model exhibit significant standby power consumption, thereby limiting their usage in the future ultralow-voltage applications. Fig. 8 depicts the RSNM and WSNM for the proposed SRAM-SDAC design comparison with 7T H-TFET SRAM cell. The proposed SRAM-SDAC was found to outperform the competing SRAM architectures.

5.2 Delay comparison

In case of differential-read SRAM cells, for example, 6T cell, the read access time (TRA) is the time required for releasing the BL and BLB voltage from its initial value after the WL is turned on amid a read operation. By a sense amplifier, the contrast amongst BL and BLB is sufficient to be detected, in this way avoiding read-upset. During single ended read operation, the read access time is the time

Table 1. Read delay comparison

Stain states (%)	0.2 V		0.3 V		0.4 V		0.5 V		0.6 V	
	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC
1.5	5n	11.912n	1n	1.2n	800p	794p	700p	729.34p	600p	690.213p
2	6n	9.129n	900p	875.12p	700p	697.12p	600p	614.564p	500p	510.193p
2.5	5n	6.87n	900p	812.102p	800p	792.0132p	600p	599.142p	500p	490.032p
3	4n	4.9894n	800p	768.029p	500p	576.372p	400p	369.2081p	100p	234.903p

Table 2. Write delay comparison

Stain states (%)	0.2 V		0.3 V		0.4 V		0.5 V		0.6 V	
	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC
1.5	10n	75.543n	7n	59.3n	6n	6.342n	5n	5.004n	4n	4.9987n
2	9n	9.23n	7n	7.218n	6.5n	6.223n	4n	4.410n	6n	3.971n
2.5	8n	8.31n	6.5n	6.280n	6n	5.909n	3n	3.109n	5n	3.213n
3	8n	7.9031n	6.5n	6.018n	6.5n	6.129n	5n	4.9087n	6n	5.346n

Table 3. Power comparison

Stain states (%)	0.2 V		0.3 V		0.4 V		0.5 V		0.6 V	
	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC	SRAM [20]	SRAM-SDAC
1.5	8.00E-13	7.60E-13	1.80E-11	9.60E-13	3.00E-12	2.68E-12	5.00E-12	4.32E-12	7.00E-12	6.90E-12
2	1.00E-12	8.12E-13	2.00E-12	1.64E-12	4.00E-12	3.90E-12	6.00E-12	5.90E-09	8.00E-12	5.09E-12
2.5	2.00E-12	1.90E-12	4.00E-12	3.42E-12	5.00E-12	4.54E-12	1.00E-11	1.79E-11	2.00E-11	1.88E-11
3	8.00E-12	6.71E-12	1.00E-11	1.41E-11	2.00E-11	2.49E-12	3.00E-11	3.19E-11	4.00E-11	3.57E-11

required for discharging the BL voltage to half of VDD after the WL is turned on. The actual read delay will be even more as it uses single ended read.

Table 1 clearly portrays the read delay of the proposed SRAM-SDAC cell is lower than SRAM cell in [20] for all strain levels. Write delay is analyzed from the writing 'Low' at node Q is the time required for node Q to fall to 10% of its initial voltage for 'High' after the WL is turned on during a write operation. Similarly, the writing 'High' is the time required for node Q to rise to 90% of voltage value for 'Low' from its initial low level after the WL is activated during a write operation. Since the core of the cell structure is similar in all the four SRAM cells during write operation, while analyzing the write access time is almost same for all SRAM cells. Table 2 clearly depicts the read delay of the proposed SRAM-SDAC cell is exceptionally lower than SRAM cell in [20] for all strain levels.

5.3 Power comparison

The power consumed by various SRAM cells while performing read and write tasks are depicted in table 3. Plainly that the proposed SRAM-SDAC cell consumes less power when contrasted with SRAM cell [20] and it consumes approximately 12% lower power as compared to others in terms of all strain states.

6. Conclusion

In this paper, we have proposed a strain and dimension effects aware (SDAC) SRAM design using TFET technologies. The proposed SRAM-SDAC design combines the new optimal depleted TFET physics model and the domino clock and input dependent (d-INDEP) low power technique to improve the performance of SRAM cell. The proposed SRAM-SDAC minimizes the both read and write delay in terms of 25% and 41% respectively. Moreover, the power consumption of proposed SRAM-SDAC design is very less in all testing scenarios. The proposed SRAM-SDAC cell is implemented in HSPICE tool with different supply voltages and strain states. The simulation results show the effectiveness of proposed SDAC design in terms of signal to noise margin, power consumption and read, write delay.

References

[1] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu, "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less

Than 60 mV/dec", *IEEE Electron Device Letters*, Vol. 28, No. 8, pp. 743-745, 2007.

[2] A. S. Verhulst, W. G. Vandenberghe, K. Maex, S. De Gendt, M. M. Heyns, and G. Groeseneken, "Complementary Silicon-Based Heterostructure Tunnel-FETs With High Tunnel Rates", *IEEE Electron Device Letters*, Vol. 29, No. 12, pp. 1398-1401, 2008.

[3] W. Choi and H. Lee, "Demonstration of hetero-gate-dielectric tunneling field-effect transistors (HG TFETs)", *Nano Convergence*, Vol. 3, No. 1, pp. 1-15, 2016.

[4] J. Nah, Y. Kim, E. S. Liu, K. M. Varahramyan, S. K. Banerjee, and E. Tutuc, "Ge-SixGe1-x core-shell nanowire tunneling field-effect transistors", *IEEE Transactions on Electron Devices*, Vol. 57, No. 8, pp. 1883-1888, 2010.

[5] J. Hur, W. Jeong, M. Shin, and Y. Choi, "Schottky Tunneling Impacts in a Tunnel FET", *IEEE Transactions on Electron Devices*, Vol. 64, No. 12, pp. 5223-5229, 2017.

[6] L. Liu, D. Mohata, and S. Datta, "Scaling Length Theory of Double-Gate Interband Tunnel Field-Effect Transistors", *IEEE Transactions on Electron Devices*, Vol. 59, No. 4, pp. 902-908, 2012.

[7] A. Mallik, A. Chattopadhyay, S. Guin, and A. Karmakar, "Impact of a Spacer–Drain Overlap on the Characteristics of a Silicon Tunnel Field-Effect Transistor Based on Vertical Tunneling", *IEEE Transactions on Electron Devices*, Vol. 60, No. 3, pp. 935-943, 2013.

[8] S. H. Kim, H. Kam, C. Hu, and T. J. K. Liu, "Germanium-source tunnel field effect transistors with record high ION/IOFF", In: *Proc. of the 2009 Symposium on VLSI Technology*, pp. 178–179, 2009.

[9] L. Lattanzio, L. D. Michielis, and A. M. Ionescu, "Complementary germanium electron-hole bilayer tunnel FET for sub-0.5-V operation", *IEEE Electron Device Lett*ers, Vol. 33, No. 2, pp. 167–169, 2012.

[10] P.-F. Guo, L.-T. Yang, Y. Yang, L. Fan, G.-Q. Han, G. Samudra, and Y.-C. Yeo, "Tunneling Field-Effect Transistor: Effect of Strain and Temperature on Tunneling Current", *IEEE Electron Device Letters*, Vol. 30, No. 9, pp. 981-983, 2009.

[11] J. Liu, M. Clavel, and M. Hudait, "Performance Evaluation of Novel Strain-Engineered Ge-InGaAs Heterojunction Tunnel Field-Effect Transistors", *IEEE Transactions on Electron Devices*, Vol. 62, No. 10, pp. 3223-3228, 2015.

[12] Q. T. Zhao, J. M. Hartmann, and S. Mantl, "An Improved Si Tunnel Field Effect Transistor With a Buried Strained Si_1-x Ge_x Source", *IEEE Electron Device Letters*, Vol. 32, No. 11, pp. 1480-1482, 2011.

[13] G. Luong, S. Strangio, A. Tiedemannn, S. Lenk, S. Trellenkamp, K. Bourdelle, Q. Zhao, and S. Mantl, "Experimental demonstration of strained Si nanowire GAA n-TFETs and inverter operation with complementary TFET logic at low supply voltages", *Solid-State Electronics*, Vol. 115, No. 2, pp. 152-159, 2016.

[14] Y. Kim, Y. Jeon, M. Kim, and S. Kim, "NOR logic function of a bendable combination of tunneling field-effect transistors with silicon nanowire channels", *Nano Research*, Vol. 9, No. 2, pp. 499-506, 2015.

[15] A. Lahgere, M. Panchore, and J. Singh, "Dopingless ferroelectric tunnel FET architecture for the improvement of performance of dopingless n-channel tunnel FETs", *Superlattices and Microstructures*, Vol. 96, No. 8, pp. 16-25, 2016.

[16] Y. Bi, K. Shamsi, J. Yuan, Y. Jin, M. Niemier, and X. Hu, "Tunnel FET Current Mode Logic for DPA-Resilient Circuit Designs", *IEEE Transactions on Emerging Topics in Computing*, Vol. 5, No. 3, pp. 340-352, 2017.

[17] B. Singh, T. Nath Rai, D. Gola, K. Singh, E. Goel, S. Kumar, P. Kumar Tiwari, and S. Jit, "Ferro-electric stacked gate oxide heterojunction electro-statically doped source/drain double-gate tunnel field effect transistors: A superior structure", *Materials Science in Semiconductor Processing*, Vol. 71, No. 15, pp. 161-165, 2017.

[18] M. Kumar and S. Park, "Improved performance of impact ionization MOSFETs by using dopingless concept and strained channel", *Superlattices and Microstructures*, Vol. 109, No. 9, pp. 763-771, 2017.

[19] K. Datta and Q. Khosru, "Simulation of thin-TFETs using transition metal dichalcogenides: effect of material parameters, gate dielectric on electrostatic device performance", *Journal of Computational Electronics*, Vol. 16, No. 2, pp. 228-239, 2017.

[20] J. Liu, M. Clavel, and M. Hudait, "An Energy-Efficient Tensile-Strained Ge/InGaAs TFET 7T SRAM Cell Architecture for Ultralow-Voltage Applications", *IEEE Transactions on Electron Devices*, Vol. 64, No. 5, pp. 2193-2200, 2017.