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FPGA Implementation of High Speed Digital FIR Filter

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ABSTRACT

Multipliers play an important role in today's digital world especially in DSP and DIP applications. With advances in technology, many researchers are trying to design multipliers which offer either of the following targets-high speed, low power consumption, regularity of layout and less area or even combination of them in one multiplier. Now-a-days researchers are focusing on low power and high speed. This may be possible by designing effective multiplies as these are involved in huge amount in almost all DSP architectures. To do so many multipliers are available such as Booth multiplier and Wallace tree multiplier. Booth multiplier gives high performance (accuracy) but with high delay, whereas Wallace tree multiplier gives high speed but with less accuracy.The proposed method of CSD multiplication has the ability to reduce truncation error, computation latency for constant word length multiplications. Furthermore Horner CSD multiplier with pipelining concept makes multiplier design power efficient and speed efficient. This novel CSD algorithm is used here to design a Digital FIR filter and the same is designed with the booth and Wallace tree algorithm and compared. It is observed that proposed design is better w.r.t no. of slices and delay in comparison with existing methods. This design is coded in Verilog HDL and targeted on the spartran-3 device of XILINX 14.5.

Keywords –**CSD (Canonic Signed Digit), DSP (Digital Signal Processing), DIP (Digital Image Processing), Verilog HDL (Hardware Description Language), VHDL (Very high speed HDL).**

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I. INTRODUCTION

The current digital world makes most works of human being just in few steps. Still delay is to be reduced along with power consumption. Delay can be reduced at various levels such as algorithmic level, architecture level, coding level, and physical level and etc. In this work architecture level is considered to design speed efficient multiplier. Here multiplier is considered on behalf of VLSI chip as it constitutes a basic component and that to contain in huge number.Popular architectures for multipliers available are Booth multiplier [10], Wallace tree multiplier [11] and CSD multiplier. Design of Simple FIR filter is considered here for illustration point of view. Booth multiplier suffers from delay, and Wallace tree multiplier suffers from accuracy. They can be overcomed with CSD multiplier.

Simple FIR filter along with Booth multiplication algorithm & Wallace Tree multiplication algorithm is discussed in Section-II, CSD multiplication algorithm for FIR filter design is discussed in Section-III, Results of these filters along with their comparison is presented in Section-IV, and conclusion of this work is presented in the last Section-V.

II. BOOTH MULTIPLIER AND WALLACE TREE MULTIPLIER FOR FIR FILTER DESIGN [10]

Architecture of FIR Filter: Direct form of FIR filter is considered in this work. This FIR filter of order M with coefficients M+1 requires M 2-input adders and M+1 multipliers. The architecture of direct form-2 FIR filter structure is as shown in Figure 1.

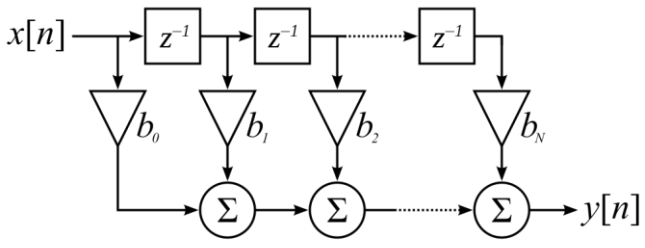

Figure 1: Direct form-2 FIR filter structure

Input output relations of a FIR filter is given by

$$y(n)=\sum_{k=0}^{M-1}h_k x(n-k) \Leftrightarrow H(z)=\sum_{k=0}^{M-1}h_k z^{-k}$$

Where x is input coefficients and h is filter coefficients. Output of the filter requires both multiplier and adder. Efficient design of these units decides overall efficiency of

Volume: 10 Issue: 02 Pages: 3800-3803 (2018) ISSN: 0975-0290

FIR filter design. For this, Booth multiplier and Wallace Tree multiplier are considered in this section and CSD multiplier case is discussed in the next section.

Booth Algorithm: This is a multiplication algorithm to multiply signed binary numbers in 2's complementary form. Step by step procedure for Booth multiplication is illustrated in Figure 2, and Hardware implementation of it is as shown in Figure 3.

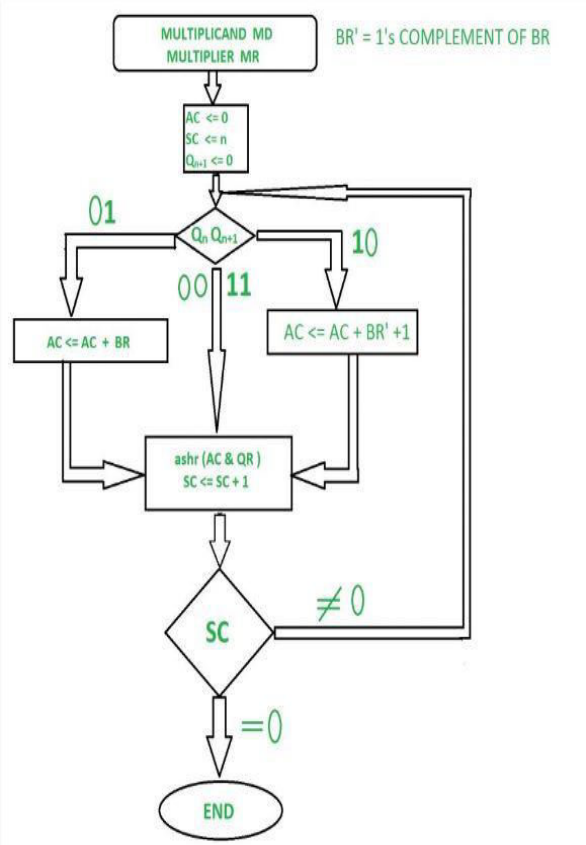

Figure 2: Flow chart for Booth Multiplication algorithm

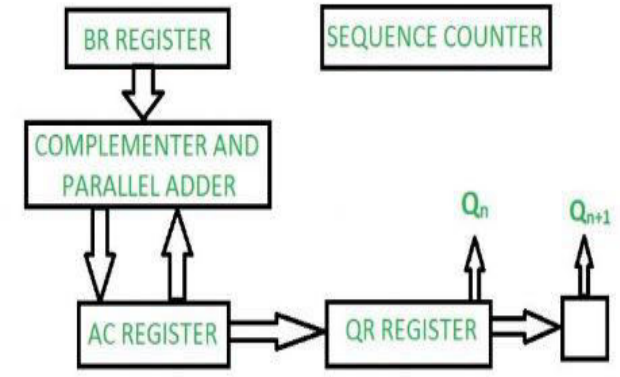

Figure 3: Hardware implementation of Booth multiplier

Wallace Multiplier: A Wallace tree is an efficient hardware implementation [11] of a digital circuit that multiplies two integers. It has 3 steps partial product generation stage, partial product reduction stage, and partial product addition stage. These are illustrated in Figure 4.

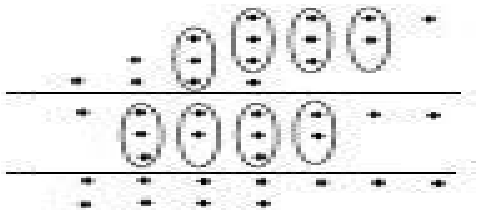

Figure 4: Wallace structure for a 4-bit multiplier

III. CSD ALGORITHM FOR FIR FILTER DESIGN

Although CSD algorithm seems to be similar to Booth algorithm, but CSD algorithm[1, 2] results in n/3 partial products instead of n/2 partial products in Booth algorithm. Hence power consumption will be further reduced with CSD algorithm. An algorithm for converting 2's complements binary number to CSD number is as shown in below and multiplication of converted CSD number with the normal binary number is as shown in Figure 5.

$$\hat{a}_{-1} = 0$$
$$\gamma - 1 = 0$$
$$\hat{a}_W = \hat{a}_{W-1}$$
$$for\ (i = 0\ to\ W-1)$$
$$\{$$
$$\theta_i = \hat{a}_i \oplus \hat{a}_{i-1}$$
$$\gamma_i = \overline{\gamma - 1}\,\theta_i$$
$$a_i = (1 - 2\hat{a}_{i+1})\gamma_i$$
$$\}$$

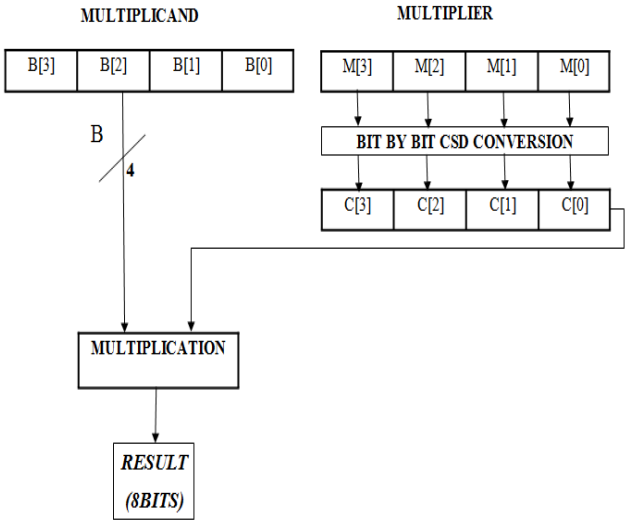

Figure 5: Pipelined CSD multiplication [3]

Volume: 10 Issue: 02 Pages: 3800-3803 (2018) ISSN: 0975-0290

IV. RESULTS & COMPARISION

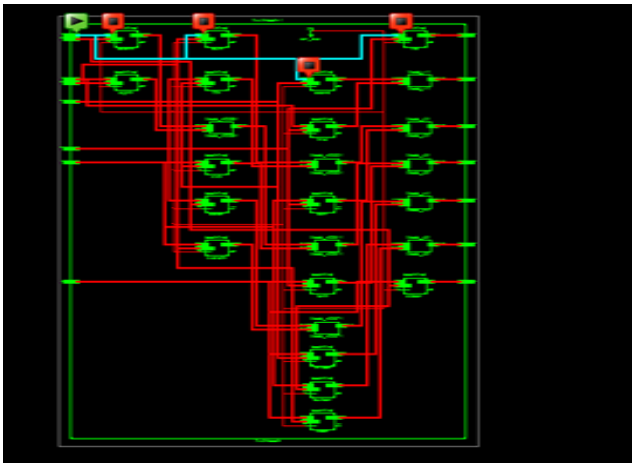

Figure 6:RTL Schematic of Booth multiplier based FIR filter

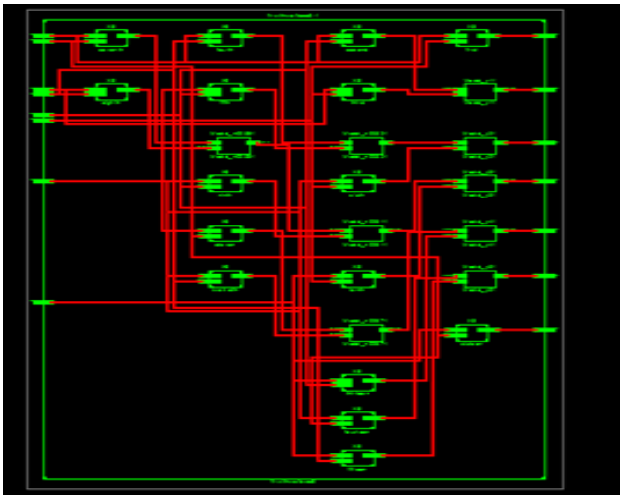

Figure 7: RTL Schematic of Wallace Tree multiplier based FIR filter

Table1: Comparision of FIR filter with different multipliers.

Parameter	FIR with Booth multiplication [10]	FIR with Wallace tree multiplication [11]	FIR with CSD multiplication
Number of slice LUTs	579/63400	3492/63400	42/63400
Number of fully used LUT- FF pairs	103/588	224/3492	0/42
Number of bonded IOBs	89/210	177/210	56/210
Delay	31.426	10.962ns	3.627ns
Memory	313604 kilobytes	345796 kilobytes	312836kilo bytes
Power consumption	42mw	42mw	42mw

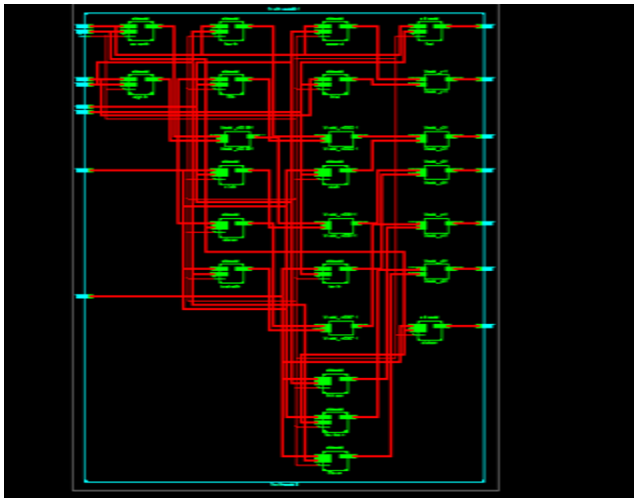

Figure 8: RTL Schematic of CSD based FIR filter

Figure 6,7 &8 shows the RTL schematic of FIR filter based on Booth multiplier, Wallacetree multiplier and CSD multiplier and corresponding synthesis results are compared in Table.1.

Table2: Delay comparison

Author	***Delay***
Mitsuru Yamada [9]	25.3ns
Abhijit Chandra [8]	30ns
Proposed	3.67ns

In this work, a new efficient FIR filter can be designed using CSD.This reduces truncation errors and delay compared with other multipliers. i.e, existing techniques requires 10ns whereas proposed technique requires 3.672ns. This method using CSD format reduces the number of add operations during multiplication. CSD multiplication reduces number of slice LUTs by 92.74% in comparison with booth multiplication.CSD multiplication reduces number of slice LUTs by 98.79 % in comparison with wallace tree multiplication.CSD multiplication reduces number of bonded IOBs by 37.07% in comparison with booth multiplication.CSD multiplication reduces number of bonded IOBs by 68.36% in comparison with wallace tree multiplication.CSD multiplication reduces delay by 66.91% in comparison with wallace tree multiplication and The method gives exact results with reduced number of add operations. Table.2 shows the comparison of existed CSD multipliers with proposed CSD multiplier and it is shown that proposed CSD multiplier is very better in terms of delay it takes.

V. CONCLUSION

In this work, a new efficient FIR filter can be designed using CSD .This reduces truncation errors and delay compared with other multipliers. This method using CSD format reduces the number of add operations during multiplication. CSD multiplication reduces number of slice LUTs in comparison with previous multiplication

Volume: 10 Issue: 02 Pages: 3800-3803 (2018) ISSN: 0975-0290

techniques. CSD multiplication reduces delay in comparison with previouswallace tree and booth multiplication techniques.This method gives exact results with reduced number of add operations.In future there existsnew design,where designers can reduce the area occupied by the adder in various technologies.This work has been designed for 8-bit word size and results are evaluated for parameters like delay and power.This work can be further extended for higher number ofbits. New architectures can be designed in order to reduce the power, area and delay of the circuits. Steps may be taken to optimize the other parameters like frequency, number of gate clocks, length etc.

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