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Design and Analysis of Row and Column Bypass multipliers using various logic Full Adders

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Abstract:

An energy efficient processor which is the key for designing is multipliers. Multipliers play an important role in DSP blocks and in many applications. The multiplication is an essential arithmetic operation for common DSP and communication application, such as filtering and FFT. "Add and Shift" algorithm is the common multiplication method. The switching activities and ower consumption is reduced by introducing the number of zeros in the multiplicand bit. This design depends on the input bit coefficient in the switching activity of the component used.

Keywords **—Multipliers, full adders, power consumption, area**.

I. INTRODUCTION

An adder in a digital circuit performs addition operation. Most of the VLSI circuits, uses adder as a critical portion since they form the base elements of all arithmetic functions[1]. In processors, adders are used as the arithmetic logic units (ALU). Adders are used to calculate addresses, table indices, increment and decrement operators, and similar operations which are applied in other parts of the processors. Using row bypassing, column bypassing and reversible logic techniques the dynamic power dissipation of the multiplier resulting from the switching activities can be decreased.

II. ROW BYPASSING

The technique which is based on number of zeros in the multiplier bits is called as row bypass technique. In the multiplier operation, the basic multiplier array of some rows of adders are disabled to save power. The structure of row bypassing adder cell is given

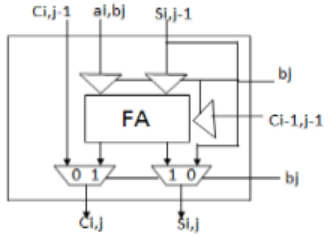

Fig. 1. Row bypass adder cell

To halt the input, three tristate buffers are added with each full adder. Tristate buffers are useful in halting the inputs when a particular full adder is bypassed. two 2:1 multiplexers are combined at sum and carry at outside to switch between normal path and bypassed path. Multiplier bits B and multiplicand A of a multiplier is considered. A simple logic to improve performance is, as soon as bj was found to be zero, that is all partial products AiBj, 0<=i<=n-1, are zero, avoid triggering those adding unit in the row to reduce power reduction a complete row is bypassed[2]. Hence, two multiplexers are required in the adding unit, in bypassing operation. ifjth bit is zero then the corresponding partial product is zero.

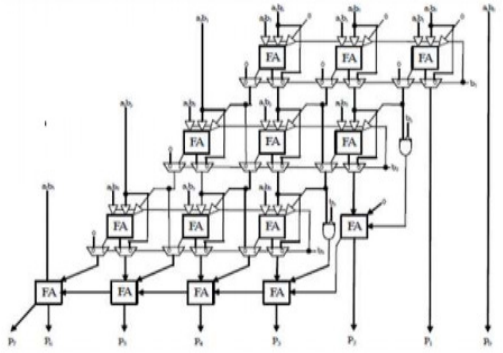

Fig.2. Structure of Row bypass multiplier.

III. COLUMN BYPASSING MULTIPLIER

There are more number of zeros in the multiplicand which decreases the number of switching activities and the power consumption in this column bypass multiplier. The component used in the switching activity design depends on the input bit coefficient. Hereby if the coefficient of the input bit is zero, the corresponding row or column of the adders need not to be activated. if the multiplicant contains more number of zeros then higher reduction power can be achieved[3]. To decrease the switching activity, the idle part of the circuit is shut down which is not in operating condition.

The total number of full adders that are required to design a column bypass multiplier are x*(x-2). In column bypass multiplier design the total number of half adders required are n.The total number of tristate buffers required to design a column bypass multiplier are 2*x*(x-1). The total number of 2 TO 1 Multiplexers required to design column bypass multiplier are (x-1)*(x-1).

In column-bypass multiplier design circuit, it is important to set the carry outputs to 0 in the bottom of the Carry Save Adder array,else the corresponding full adders may not produce the correct outputs because their inputs are disabled. This is done by adding an AND gate at the outputs of the last-row Carry Save Adder. The structure of column bypassing adder cell is,

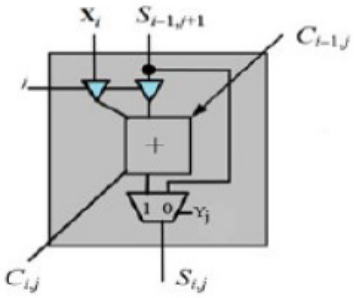

Fig.3. Column bypass adder cell

The structure of column bypass multiplier is,

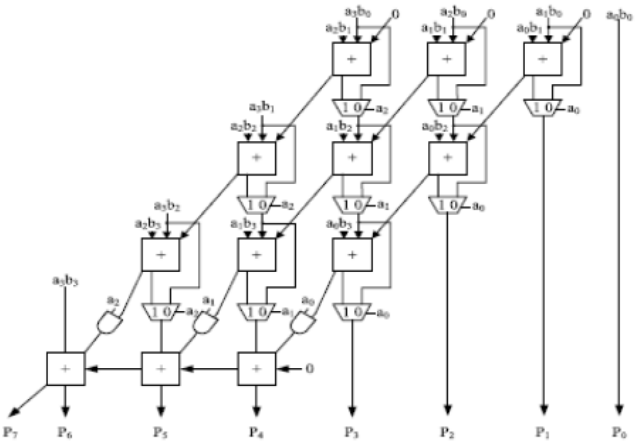

Fig.4. Structure of Column bypass multiplier

IV. ANALYSIS OF ROW AND COLUMN BYPASS MULTIPLIER

A. 8T full adder based Row and Column bypass multiplier

8T Full Adder method is based on the operation of a simple cell. XOR and XNOR functions are the key variables in adder equations.to greatly enhance the performance of the full adder cell their generation should be optimized. The Boolean equation for 8T full adder design is as follows,

SUM = A(xor)B(xor)C
CARRY = AB+BC+CA

By cascading the exclusive OR of 3 inputs, the sum output is achieved. According to the Boolean equation, the carry output is achieved. The final sum product is obtained using wired OR logic[4]. At most two stage delays are essential to obtain the carry output and delays of 2 stages are resulted for sum output. This design is best on threshold loss, power dissipation and delay.

The simulation of 8T Full Adder is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of 8T Full Adder cell is shown in Fig.5 and Fig.6 respectively.

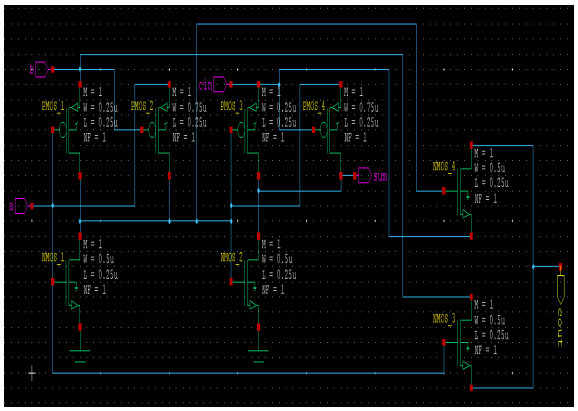

Fig.5. S-edit schematic cell of 8T full adder

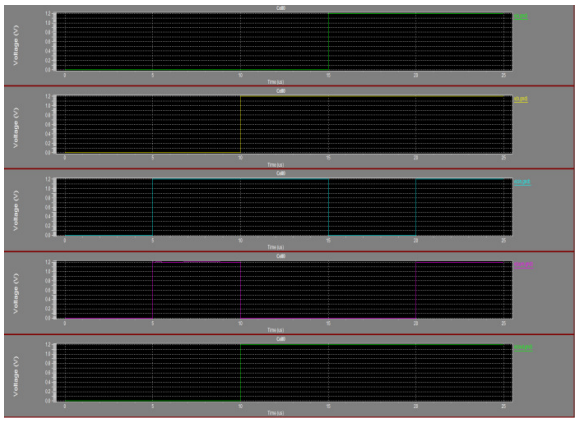

Fig.6. W-edit output waveform of 8T full adder

The simulation of Column bypass multiplier using 8T Full Adder is performed in Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform is shown in Fig7 and Fig.8 respectively.

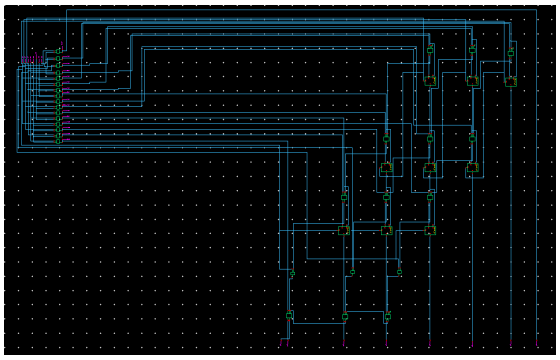

Fig.7. S-edit schematic cell of 8T Column bypassing full adder

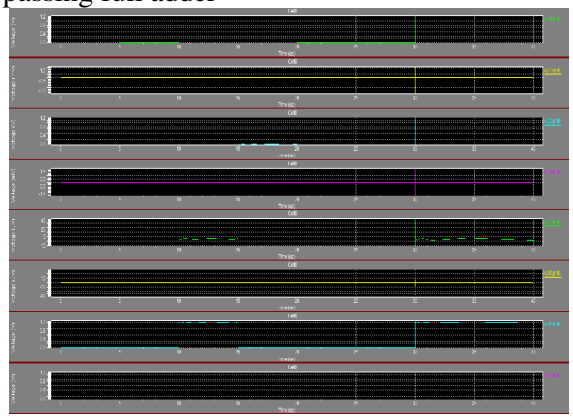

Fig.8. W-edit output waveform of 8T Column bypassing full adder

The simulation of Row bypass multiplier using 8T Full Adder is performed in Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform is shown in Fig9 and Fig.10 respectively.

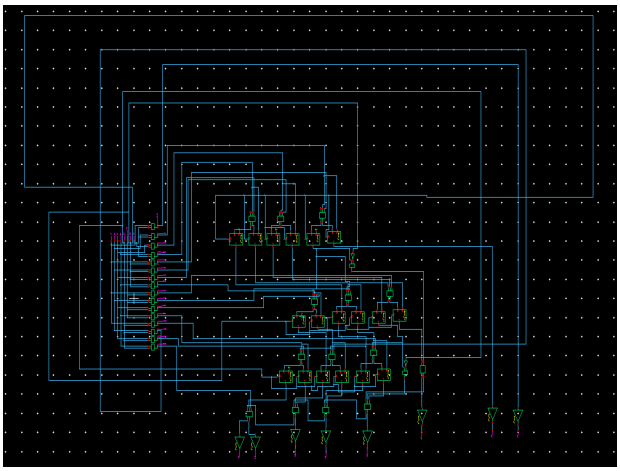

Fig.9. S-edit schematic cell of 8T Row bypassing full adder

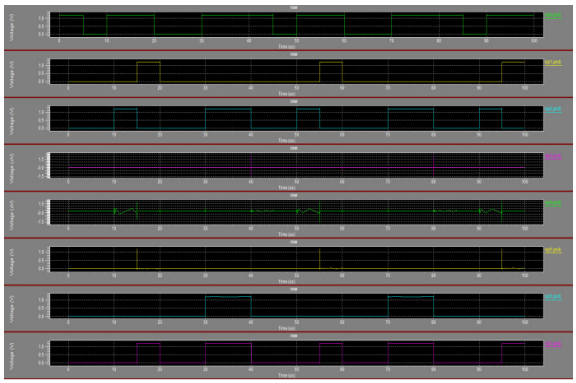

Fig.10. W-edit output waveform of 8T Row bypassing full adder

A. 10T full adder based row and column bypass multiplier

Here, CMOS logic implemented using 10T. In this circuit, V_{DD} and GND connections are inclined. This design shows the comparative study of advancement with power supply over active power leakage current and delay[5]. Full adder is compared with the other circuits and 10T is presented with the same.

The simulation of 10T Full Adder is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of 10T Full Adder cell is shown in Fig.11andFig.12
respectively

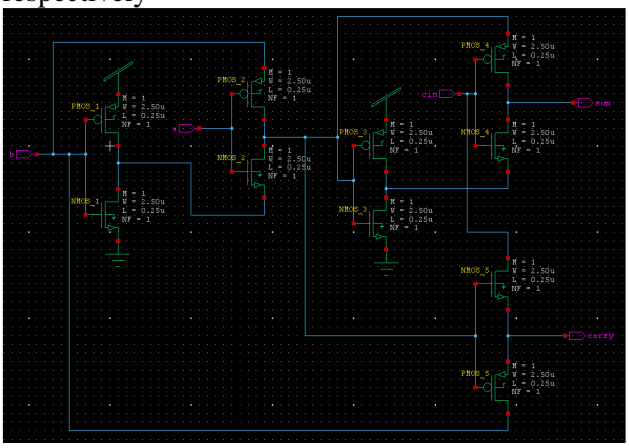

Fig.11. S-edit schematic cell of 10T full adder.

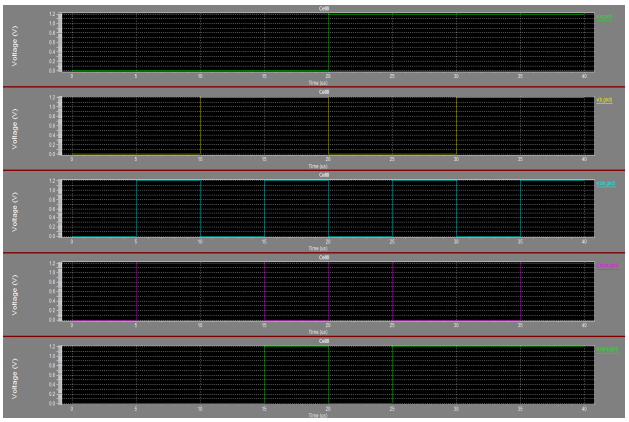

Fig.12. W-edit output waveform of 10T Row bypassing full adder.

The simulation of Column bypass multiplier using 10T Full Adder is performed in Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform is shown in Fig.13 and Fig.14 respectively.

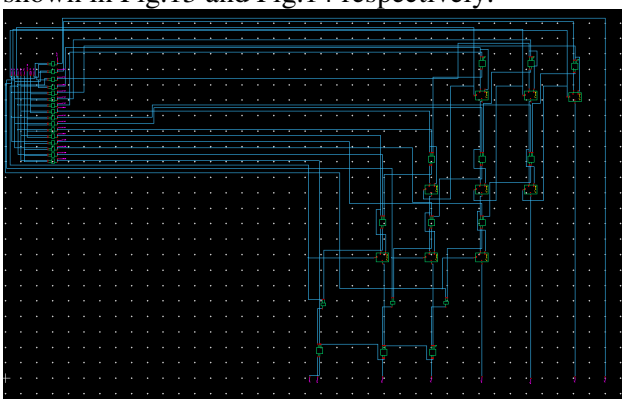

Fig.13. S-edit schematic cell of 10T Column bypassing full adder.

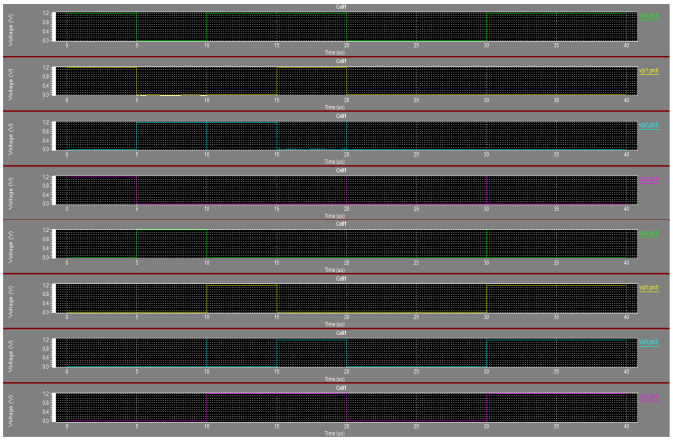

Fig.14. W-edit output waveform of 10T Column bypassing full adder.

The simulation of Row bypass multiplier using 10T Full Adder is performed in Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform is shown in Fig15 and Fig.16 respectively.

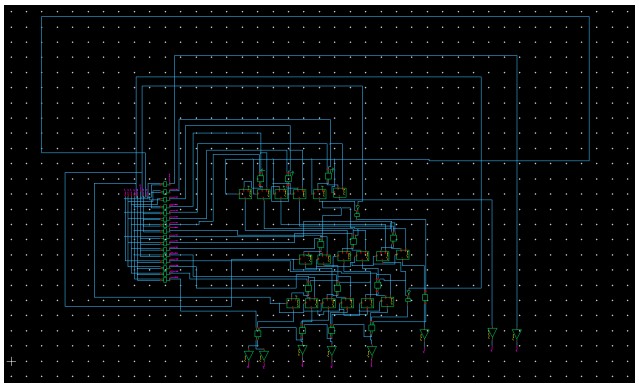

Fig.15. S-edit schematic cell of 10T Row bypassing full adder.

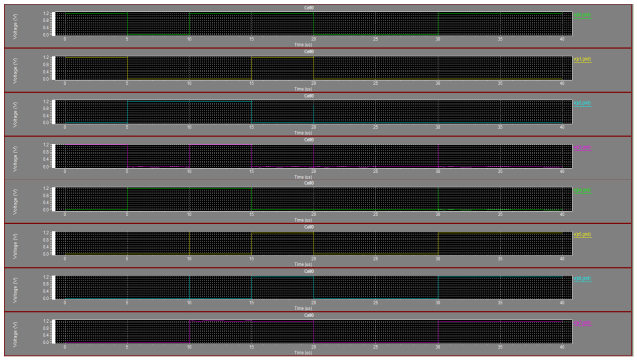

Fig.16. W-edit output waveform of 10T Row bypassing full adder.

B. 12T full adder based row and column bypass multiplier

With six multiplexers and 12 transistors, 12T is implemented. The implementation of each multiplexer is performed by pass transistor logic with two transistors. There is no power supply and ground connection in this circuit. There are some paths containing three serried transistors[6] . The SUM signal is obtained by increasing the delay. Area of the circuit is increased due to transistor size in the mentioned path should be three times larger to balance the output and optimize the circuit for PDP.

The simulation of 12T Full Adder is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of 12T Full Adder cell is shown in Fig.17 and Fig.18 respectively.

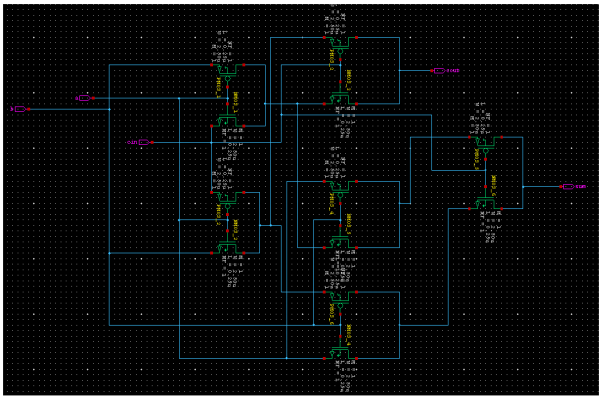

Fig.17. S-edit schematic cell of 12T full adder

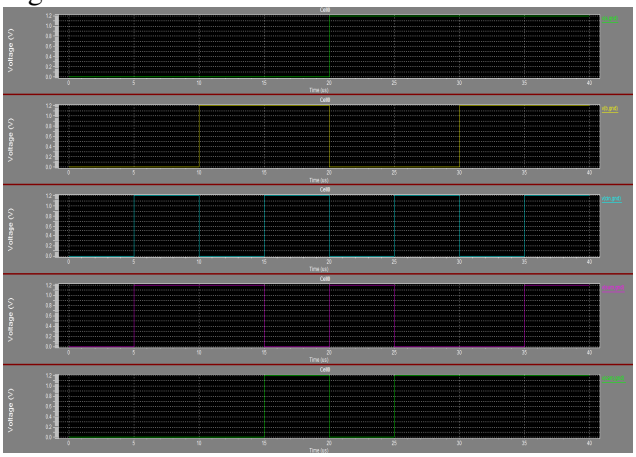

Fig.18. W-edit output waveform of 12T full adder.

The simulation of Column bypass multiplier using 12T Full Adder is performed in Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform is shown in Fig.19 and Fig.20 respectively.

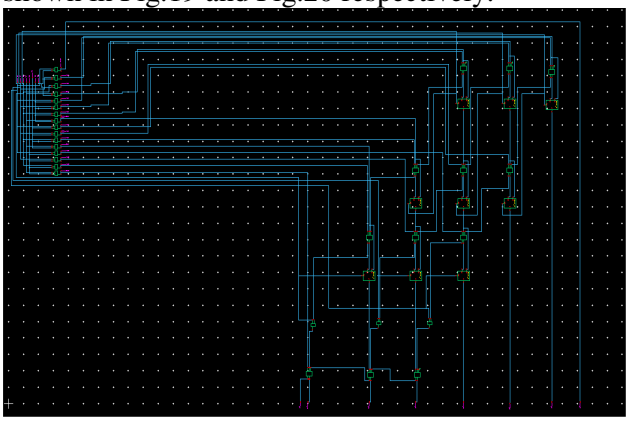

Fig.19. S-edit schematic cell of 12T Row bypass full adder.

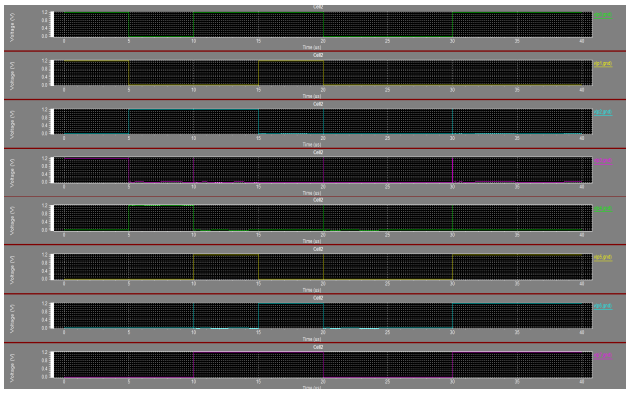

Fig.20. W-edit output waveform of 12T Row bypass full adder.

The simulation of Row bypass multiplier using 12T Full Adder is performed in Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform is shown in Fig21 and Fig.22 respectively.

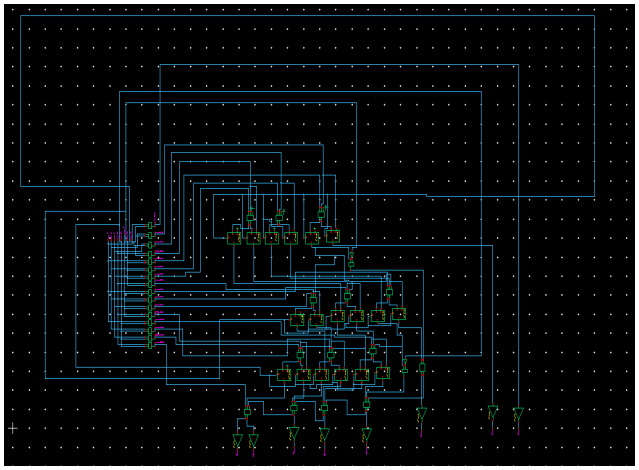

Fig.21. S-edit schematic cell of 12T Row bypass full adder.

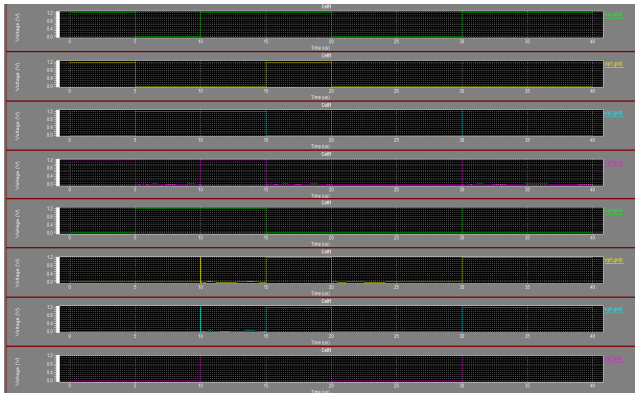

Fig.22. W-edit output waveform of 12T Row bypass full adder.

V. SIMULATION RESULTS AND COMPARISON

Simulations are performed using Tanner EDA using 130nm technology nodes. The analysis shows reduced power, delay, PDP, area and transistor count for proposed row bypass multiplier using 8T full adder is compared with row bypass multiplier using 10T, 12T full adders. The simulation results of column bypass multiplier are tabulated in table 1 and simulation results of row bypass multiplier are tabulated in table 2.

TABLE I
SIMULATION RESULTS AND COMPARISON

Parameters	Various Column Bypass Multipliers		
	8T	10T	12T
Power (µW)	35	49	63
Delay (µS)	0.9	1.2	1.6
PDP (pJ)	31.5	58.8	100.8
Area (µm²)	51.75	273.35	288.75
No.of.transistors	414	438	462

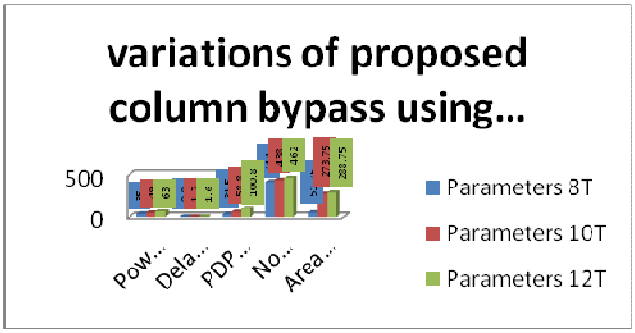

Fig.23 Variations of proposed column bypass multipliers using various logic full adders.

TABLE III
SIMULATION RESULTS AND COMPARISON

Parameters	Various Row Bypass Multipliers		
	8T	10T	12T
Power (µW)	23.69	38.26	48.25
Delay (µS)	1.6	2.2	2.6
PDP (pJ)	37.90	84.17	125.45
Area (µm²)	74.25	387.5	403.75
No.of.transistors	594	620	646

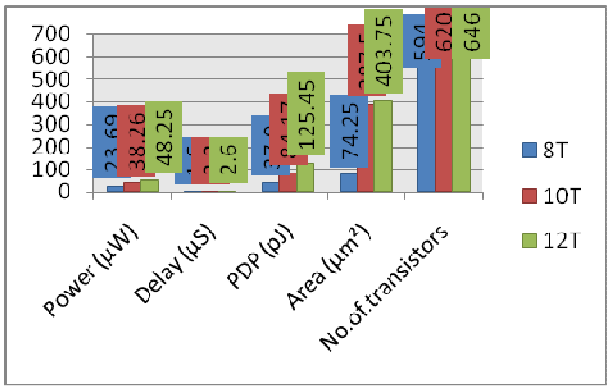

Fig.24 Variations of proposed column bypass multipliers using various logic full adders.

VI. CONCLUSIONS

Various adders were surveyed based on their architecture which involves transistor count. Row and column bypass multipliers were designed using full adders namely 8T, 10T and 12T. The parameters like area, power, delay, PDP were analyzed. Simulations were performed with the help of Tanner EDA using 130nm technology nodes. The same logic can be implemented in higher architecture for desired output in future.

ACKNOWLEDGMENT

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