Research Article

Effects of Device Parameter Variation in Low-Voltage Digital and Analog Circuits

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ABSTRACT

In this paper, a closed-form model for device variability has been derived to study the impact of device parameter variations on low-voltage mixed signal circuits. Based on this model, a projected 22nm technology is used to examine the effects of device parameter variation on both digital and analog circuits. For digital circuit, delay (t_{PHL}) variation, noise margin (NM_H and NM_L) variation for an inverter are investigated. Current variation of a current mirror, gain variation of a differential operational amplifier are considered for analog circuit analysis. Analytical simulation results suggest that, in most cases, overall variation increases as the supply voltage in digital circuits or overdrive voltage in analog circuit decreases. Analytical results also show that, NM_H variation in a digital circuit is more sensitive to the process related issues than NM_L variation. Moreover, nominal value for NM_H is higher than nominal value of NM_L when supply voltage is more than 0.8V.

Keywords: Analog Circuits, Digital Circuits, Low-Power, Low-Voltage, Mixed-Signal Circuits, Noise Margin, Process Parameters variations.

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INTRODUCTION

As research in ultra-low-power circuit design advances, a vision of highly integrated mobile computing systems with lifetimes in the order of years is emerging. Such computing systems are attractive for biomedical implants, supply chain management, and environmental monitoring. The energy consumption of these systems ultimately limits form factor, battery life, and complexity. Therefore, developing circuits that can perform complex tasks under stringent energy constraints is very important [1]. Over the past several decades, a large number of digital design techniques have been explored that can perform efficiently under low power supplies. However, scaling of supply voltage is considered as the most effective solution to stringent power requirements since it results in a quadratic reduction of dynamic power [2]. Very low-voltage operation of VLSI's is effective in reducing both dynamic and leakage power while achieving maximum energy efficiency. However, this down scaling of the supply voltage is done at the expense of design performance and efficiency.

The process variability in integrated circuits which has been previously demonstrated in several work is an important issue for low voltage circuits [3-5]. The effect in nanometer-scaled circuits causes significant deviation from the prescribed specification for a chip. The magnitude of the deviations together with tight performance specifications, imply that variability is an increasingly vexing problem as technologies continues to scale. Process related variations are one-time variations that occur when a circuit is manufactured and cause process parameters to drift from their design values [5]. This variation can impact key circuit performance characteristics: for digital circuits, the effected parameter includes the delay, noise margin and logic threshold of the circuit; while for analog circuits, the performance parameters to be monitored are specific to the type of circuit. It is increasingly obvious that designing circuit at the nominal point, or using simple corner based approaches, are no longer viable [5]. As a result, properly analyzing the effect of process related variation on digital and analog circuit has become the most demanding concern. To do so, an analytical model is required and a closed-form model for device variability is derived in this paper to enable first order estimation of some fundamental circuit parameters. This analysis can be extended to develop models for the impact of variations on any circuit/system's parameters.

The paper consists of three main sections. Section I describes a *device variation map* that was first proposed by Bernstein *et al* in 2006 using experimental data. In this section a device variation map is constructed by using ana-

lytical models. An example of a projected device variation map is shown for a 22nm CMOS process from predictive technology model (PTM) [2,6,7]. In section II, a device variation map and some new analytical models are used to analyze the effects of device parameter variation on digital circuits that have low supply voltage. The effects on low voltage analog circuits are shown in the following section III, using analytical models.

Analysis on this paper places strong emphasis on ultra-low voltage circuits operating in super threshold region only.

I. DEVICE VARIATION MAP

Bernstein *et al* was first to use experimental and measured data to illustrate device variations by using a color map. They have used an I-V characteristics plot of a 65nm CMOS device. The color map has been shown in Figure 1[2]. The background color in the figure is indexed to the magnitude of device current variation [2]. This device's current variation was observed in DC hardware characterization of the CMOS device. Device was operated at the specific drain-source voltage (V_{DS}), drain-source currents (I_{DS}) and implied gate-source voltage (V_{GS}) point on the plot. The highest and lowest device current variation areas are marked as red and blue colors respectively. To estimate the impact of device variations on various circuit topologies, this color map shown in Figure 1 will turn out as a very handy tool. We have developed analytical models to construct such a device variation map for any given technology node [2]. Our derived analytical models are presented in details in flowing sub-sections.

A. Assumptions

It is difficult to ensure a firm parameter value for all devices during IC fabrication process. All device parameters are subject to deviate from their nominal values. In this work, attention has been given to a limited number of transistor parameters such as threshold voltage (ΔV_t), effective channel length (ΔL_{eff}) and device width (ΔW). Statistical models have been developed considering only these parameters as variables. However, these methods can be extended to any additional variables as well [2].

B. Derivation

In general, the drain-source current, I_{DS} of a transistor is represented by:

$$I_{DS} = f(V_t, L, W) \tag{1}$$

Where V_t is the threshold voltage, L is the device length and W is the device width. Function f can be any analytical model that describes the device characteristics, such as alpha-power law model [8], unified mode l [9] or MOSFET transregional model [10], where it covers all regions of operations including the sub-threshold region [2].

With the assumption that device variations are small compared to their nominal value and they can be approximated by Gaussian distribution. The device current variation can be derived by taking partial derivative as shown below:

$$\Delta I_{DS} = \sqrt{(\frac{\partial f}{\partial V_t})^2 \Delta V_t^2 + (\frac{\partial f}{\partial L})^2 \Delta L^2 + (\frac{\partial f}{\partial W})^2 \Delta W^2} \tag{2}$$

Here, each term represents contribution of variation to the associated device parameter such as threshold voltage, effective channel length, and device width. To simplify the derivation, the unified model is used to represent the transistor drain-source current, I_{DS} :

$$I_{DS} = K_n' \left(\frac{W}{L}\right) \left((V_{GS} - V_t) V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \tag{3}$$

Where $V_{min} = min\{(V_{GS} - V_t), V_{DS}, V_{DSAT}\}$, V_{DSAT} is the drain-source voltage under velocity saturation, K_n' is the device trans conductance, λ is the channel length modulation factor and (W/L) is the device aspect ratio. From partial derivative equation in (2) the device current variation can be derived and simplified as [2]:

$$\frac{\Delta I_{DS}}{I_{DS}} = \sqrt{\left(\frac{2\Delta V_t}{2(V_{GS} - V_t)V_{min}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2} \tag{4}$$

Where $V_{min} = min\{(V_{GS} - V_t), V_{DS}, V_{DSAT}\}$.

Table -1 The PTM's 22nm CMOS Device Parameters [2]

Device	V_t	K'	V_{DSAT}	λ	(W/L)	% ΔV_t	% ΔW	% ΔL_{eff}	% ΔV_{DD}
NMOS	0.37 V	97.5 $\mu A/V^2$	0.24 V	0.06 V^{-1}	100	4%	1.2%	2.5%	5%
PMOS	0.25 V	12.0 $\mu A/V^2$	0.75 V	0.1 V^{-1}	200	4%	1.2%	2.5%	5%

A similar device variation map of Fig. 1 can be generated by using the analytical model represented in (4). Device variation map for a projected 22nm CMOS is shown in Fig. 2, as an example. Similarity in device variation trends are clearly noticeable in these figures.
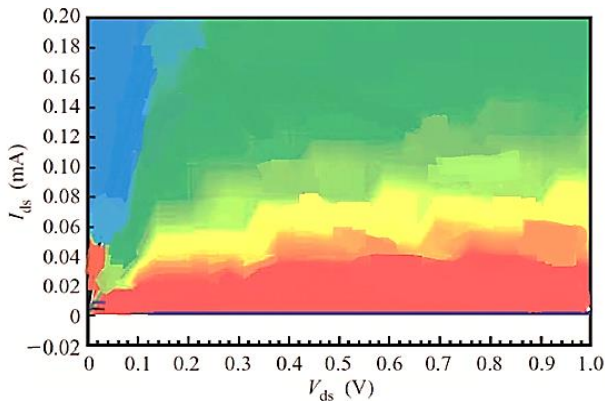
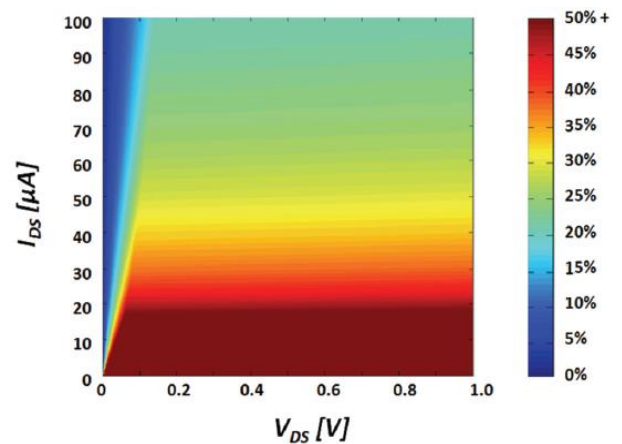Fig. 1 Device variation map on a 65nm NMOS I-V characteristics using experimental data [2]

Fig. 2 Projected Device Variation map for PTM's 22nm NMOS Device [2]
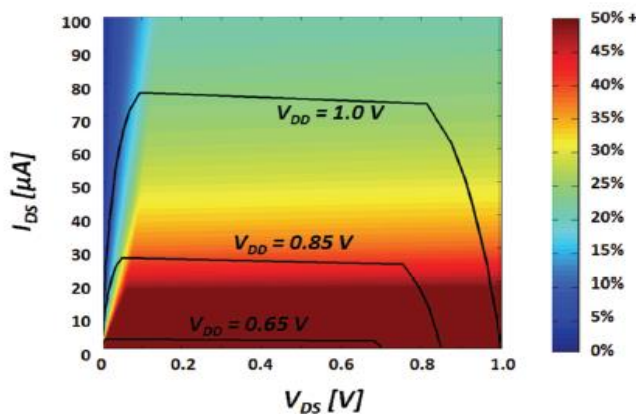

Fig. 3 The I-V trajectory of an NMOS in an inverter under different supply voltages using PTM's 22n m device parameters [2]
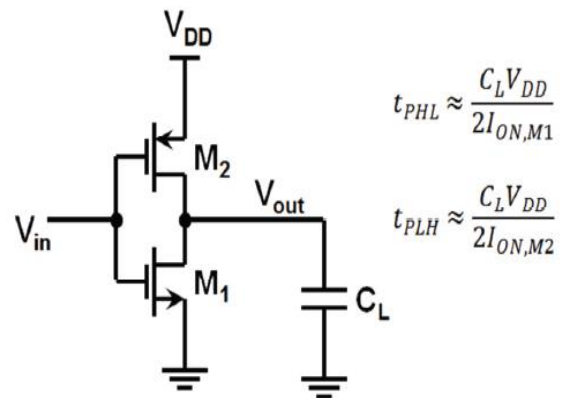

Fig.4 An Inverter circuit and the simplified delay model, assuming the transistor stays the saturation during the transition [2]

$$t_{PHL} \approx \frac{C_L V_{DD}}{2 I_{ON,M1}}$$

$$t_{PLH} \approx \frac{C_L V_{DD}}{2 I_{ON,M2}}$$

II. LOW VOLTAGE DIGITAL CIRCUITS UNDER DEVICE VARIATIONS

Analytical model for device variation map that we have derived in previous section is the key element to analyze the impact of device variations for electronic circuits. For example, Figure 3 illustrates the I-V trajectory of a NMOS in an inverter under different supply voltages. Parameter values for the NMOS are taken from the PTM's 22nm CMOS technology node. Details of parameter's nominal values and percentage of variations for each parameter are described in Table -1. Figure 3 clearly illustrates that the impact of device variations becomes severe in inverters as supply voltages goes lower, because the device spent a larger portion of the trajectory in the high (red) variation region [2].

A. Propagation Delay

A similar approach of section II has been used here to derive an analytical model for quantifying the impact of device variations on the delay of a digital circuit. High-to-low propagation delay (t_{PHL}) of a circuit can be represented by a function, 'g' as following [2]:

$$t_{pHL} = g\,(V_{DD}, V_t, L, W) \tag{5}$$

Assuming that the variation of device parameters is small compared to their nominal values and they can be approximated by the Gaussian distribution, the inverter delay variation can derive by taking partial derivatives as shown in [2]:

$$\Delta t_{PHL} = \sqrt{\left(\frac{\partial g}{\partial V_{DD}}\right)^2 \Delta V_{DD}^2 + \left(\frac{\partial g}{\partial V_{t,n}}\right)^2 \Delta V_{t,n}^2 + \left(\frac{\partial g}{\partial L}\right)^2 \Delta L^2 + \left(\frac{\partial g}{\partial W}\right)^2 \Delta W^2} \tag{6}$$

Here each term represents the contribution of the variation to the associated device parameter. To simplify the derivation, we have assumed that, NMOS transistor is in velocity saturation region during high-to-low propagation of output. Figure 4 shows the circuit diagram of an inverter. A simplified delay model can be rewritten as:

$$t_{PHL} \approx \frac{C_L}{2} * \frac{V_{DD}}{I_{ON}} \approx \frac{C_L V_{DD}}{k_n'\left(\frac{W}{L}\right)_n \{(V_{DD}-V_{t,n})V_{DSAT,n} - \frac{V_{DSAT,n}^2}{2}\}} \tag{7}$$

From partial derivative equation in (6) the inverter delay variation can be derived and simplified as:

$$\frac{\Delta t_{PHL}}{t_{PHL}} = \sqrt{\left(\frac{V_{DSAT,n}+2V_{tn}}{2V_{DD}-2V_{tn}-V_{DSAT,n}} \cdot \frac{\Delta V_{DD}}{V_{DD}}\right)^2 + \left(\frac{2\Delta V_{tn}}{2V_{DD}-2V_{tn}-V_{DSAT,n}} \cdot\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2} \tag{8}$$

In addition, the variation of low-to-high propagation delay can be modeled by an equation analogous to (8). Using the device parameters for 22nm technology node given in Table -1 and the analytical model in (8), the plot of delay variation components versus supply voltage is illustrated in Figure 5. As expected, reducing supply voltage results in a very large delay variation. However, the analytical model shown in (8) provides the contribution of each variability component separately.

Figure 5 shows that, for analytical model presented in (8), V_{DD} and V_t are dominant source of uncertainty, especially when supply voltage is reduced below 0.8V. According to Figure 5, the impact of channel length and device width variations are negligible on delay variation in digital circuits.

For 0.62V supply voltage(V_{DD}), total variation is 22.2% where major contribution comes from V_{DD} variation (18.9%). 4% of V_t variation creates 11.4% of delay variation in an inverter operating at 0.62V. It is important to note that, delay variation due to L variation and W variation do not vary with the supply voltage. Contribution of L variation is fixed at 2.5% and W variation contributes only 1.2%. At V_{DD} =1V, total variation is around 6% only. However, Total variation becomes more than 20% when V_{DD} reaches around 0.62V.
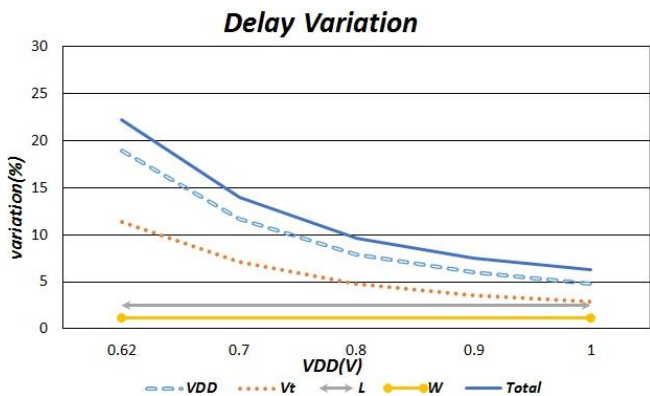

Fig. 5 Delay variation versus supply voltage for an inverter in PTM's 22nm technology node [2]

Table -2 Operational Region of Transistors in an Inverter

Region	Input Voltage V_I	Output		NMOS	PMOS
1	$V_I \leq V_{t,n}$	Voltage V_o		Transistor	Transistor
		$V_{OH} = V_{DD}$	Cutoff	Linear
2	$V_{t,n} < V_I \leq V_o + V_{t,p}$	High		Saturation	Linear
3	$V_o + V_{t,n} < V_I \leq (V_{DD} + V_{t,p})$	Low		Linear	Saturation
4	$V_I \geq (V_{DD} + V_{t,p})$	$V_{OL} = 0$		Linear	Cutoff

B. Noise Margin (High State) Variation

Unwanted signals, such as noise, must be addressed in any system of logic, particularly in ultralow-power CMOS. The noise margin is the difference between a valid output logic level and an input level at which the data of a ''victim'' circuit will be corrupted. (A victim circuit is one that is subject to noise from an external source) [3].

A vital way to investigate the impact of device parameter variations in the digital circuit is to analyze the noise margin variations; both NM_L and NM_H. Operational region of a transistor in an inverter for our case, is given in table-2:

Equating currents for linear NMOS transistor and saturated PMOS transistor (Region 3), we can find the following result: - $\frac{k_n}{2}\left[2\left(V_{IH}-V_{t,n}\right)V_{out}-V_{out}^2\right]=\frac{k_p}{2}\left(V_{DD}-V_{IH}-|V_{t,p}|\right)^2$

The derivation condition $(dV_{out}/dV_{in}) = -1$ has to be evaluated. Assuming, $V_{out} = 0$ and $V_{in} = V_{IH}$

$$V_{IH} = \frac{V_{DD}-|V_{t,p}|+V_{t,n}*K_R}{1+K_R}$$

Here, $K_R = \frac{K_n}{K_p} = \frac{K_n'}{K_p'} * \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p}$

After making some simplifications on above equation of V_{IH} and assuming that, $V_{OH}=V_{DD}$; a simplified equation for Noise margin (High State), NM_H can be written as follows:

$$NM_H = V_{OH} - V_{IH} = \frac{V_{DD}*K_R+|V_{t,p}|-V_{t,n}*K_R}{1+K_R} \tag{9}$$

Assuming that the variation of the device parameters is small compare to their nominal values and they can be approximated by Gaussian distribution, device NM_H variation can be derived by taking the partial derivative and the equation is as following:

$$\frac{\Delta NM_H}{NM_H} = \sqrt{\frac{(\frac{\partial NM_H}{\partial V_{DD}})^2 * \Delta V_{DD}^2 + (\frac{\partial NM_H}{\partial V_t})^2 * \Delta V_t^2 + (\frac{\partial NM_H}{\partial L})^2 * \Delta L^2 + (\frac{\partial NM_H}{\partial W})^2 * \Delta W^2}{(\frac{V_{DD}*K_R+|V_{t,p}|-V_{t,n}*K_R}{1+K_R})^2}} \tag{10}$$

Where,

(a) $\frac{\partial NM_H}{\partial V_{DD}} * \Delta V_{DD} = \frac{K_R}{1+K_R} * \Delta V_{DD}$

(b) $\frac{\partial NM_H}{\partial V_t} * \Delta V_t = \sqrt{\left(\frac{\partial NM_H}{\partial V_{t,p}} * \Delta V_{t,p}\right)^2 + \left(\frac{\partial NM_H}{\partial V_{t,n}} * \Delta V_{t,n}\right)^2} = \sqrt{\left(\frac{1}{1+K_R} * \Delta V_{t,p}\right)^2 + \left(\frac{-K_R}{1+K_R} * \Delta V_{t,n}\right)^2}$

(c) $\frac{\partial NM_H}{\partial L} * \Delta L = \sqrt{\left(\frac{\partial NM_H}{\partial L_n} * \Delta L_n\right)^2 + \left(\frac{\partial NM_H}{\partial L_p} * \Delta L_p\right)^2} = \sqrt{\left(\frac{\frac{K_R(V_{t,n}+|V_{t,p}|-V_{DD})}{L_n}}{(1+K_R)^2} * \Delta L_n\right)^2 + \left(\frac{\frac{K_R(V_{DD}-|V_{t,p}|-V_{t,n})}{L_p}}{(1+K_R)^2} * \Delta L_p\right)^2}$

(d) $\frac{\partial NM_H}{\partial W} * \Delta W = \sqrt{\left(\frac{\partial NM_H}{\partial W_n} * \Delta W_n\right)^2 + \left(\frac{\partial NM_H}{\partial W_p} * \Delta W_p\right)^2} = \sqrt{\left(\frac{\frac{K_R(V_{DD}-|V_{t,p}|-V_{t,n})}{W_n}}{(1+K_R)^2} * \Delta W_n\right)^2 + \left(\frac{\frac{K_R(V_{t,n}+|V_{t,p}|-V_{DD})}{W_p}}{(1+K_R)^2} * \Delta W_p\right)^2}$

Figure 6 shows that, for analytical model shown in (10), nominal value of *NM_H* decreases with the reduced supply voltage. For 0.8V supply voltage nominal value is 394mV and for 1V supply voltage noise margin increases to 555mV. Noise margin is 475mV when V_{DD}=0.9V.

On the other hand, total *NM_H* variation due to process related issues, increases as the supply voltage reduces. *NM_H* variation increases from 7.56% to 8.7% when V_{DD} reduces from 1V to 0.8V. Following table illustrates the individual contribution of each parameter variation on overall *NM_H* variation. It is clear from the table that, V_{DD} variation and V_t variations play key roles in overall *NM_H* variation. *NM_H* variation due to both of them increases as V_{DD} increases. For V_{DD} =0.8V, V_{DD} variation contribution is roughly 3X more than the contribution of V_t variation. Like delay variation, contribution of *L* and *W* variations are not so important and they are less than 1% when V_{DD} varies in between 0.8V and 1V range. For V_{DD}= 1V, *NM_H* variations due to V_t variation is 2.17% and for V_{DD} =0.8V, it is 3.05%. For same voltages *NM_H* variation due to V_{DD} variations are 7.23% and 8.14% respectively.
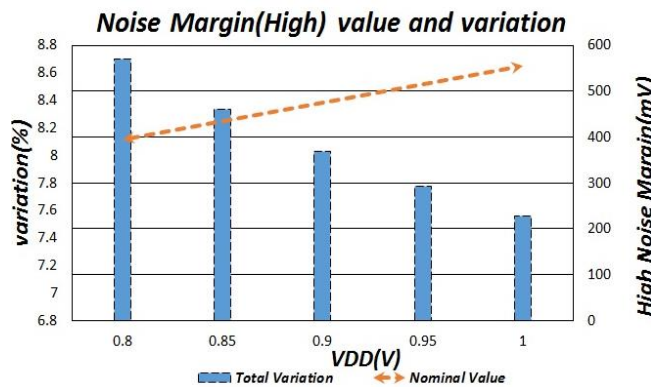

Fig.6 *NM_H* variation versus supply voltage for an inverter in PTM's 22nm technology node

Table -3 Noise Margin (High State) Variation

	NM (High) Variation (%)					
VDD(V)	VDD	Vt	L	W	Total	NM(mV)
0.8	8.14	3.05	0.26	0.12	8.697	394
0.85	7.85	2.77	0.3	0.14	8.331	435
0.9	7.61	2.54	0.33	0.16	8.031	475
0.95	7.4	2.34	0.36	0.17	7.771	515
1	7.23	2.17	0.38	0.18	7.56	555

C. Noise Margin (Low State) Variation

Equating currents for saturated NMOS transistor and linear PMOS transistor (Region 2)

$$\frac{k_n}{2}\left(V_{in}-V_{t,n}\right)^2 = \frac{k_p}{2}[2\left(V_{DD}-V_{in}-|V_{t,p}|\right)(V_{DD}-V_{out})-(V_{DD}-V_{out})^2]$$

The derivation condition $(dV_{out}/dV_{in}) = -1$ has to be evaluated. Assuming, $V_{out} = V_{DD}$ and $V_{in} = V_{IL}$

$$V_{IL} = \frac{V_{DD}-|V_{Tp}|+V_{Tn}*K_R}{1+K_R} \qquad \text{Here,} \qquad K_R = \frac{K_n}{K_p} = \frac{K_n'}{K_p'} * \frac{(\frac{W}{L})_n}{(\frac{W}{L})_p}$$

After making some simplifications on above equation of V_{IL} and assuming that, V_{OL}=0; a simplified equation for Noise margin (Low State), *NM_L* can be written as follows:

$$NM_L = V_{IL} = \frac{V_{DD}-|V_{Tp}|+V_{Tn}*K_R}{1+K_R} \tag{11}$$

Assuming that the variation of the device parameters is small compare to their nominal values and they can be approximated by Gaussian distribution, device NM_L variation can be derived by taking the partial derivative and the equation is as following:

$$\frac{\Delta NM_L}{NM_L} = \sqrt{\frac{(\frac{\partial NM_L}{\partial V_{DD}})^2 * \Delta V_{DD}^2 + \left(\frac{\partial NM_L}{\partial V_T}\right)^2 * \Delta V_T^2 + \left(\frac{\partial NM_L}{\partial L}\right)^2 * \Delta L^2 + \left(\frac{\partial NM_L}{\partial W}\right)^2 * \Delta W^2}{(\frac{V_{DD} - |V_{Tp}| + V_{Tn} * K_R}{1+K_R})^2}} \tag{12}$$

Where,

(a) $\dfrac{\partial NM_L}{\partial V_{DD}} * \Delta V_{DD} = \dfrac{1}{1+K_R} * \Delta V_{DD}$

(b) $\dfrac{\partial NM_L}{\partial V_t} * \Delta V_t = \sqrt{\left(\dfrac{\partial NM_L}{\partial V_{t,p}} * \Delta V_{t,p}\right)^2 + \left(\dfrac{\partial NM_L}{\partial V_{t,n}} * \Delta V_{t,n}\right)^2} = \sqrt{\left(\dfrac{-1}{1+K_R} * \Delta V_{t,p}\right)^2 + \left(\dfrac{K_R}{1+K_R} * \Delta V_{t,n}\right)^2}$

(c) $\dfrac{\partial NM_L}{\partial L} * \Delta L = \sqrt{\left(\dfrac{\partial NM_L}{\partial L_n} * \Delta L_n\right)^2 + \left(\dfrac{\partial NM_L}{\partial L_p} * \Delta L_p\right)^2} = \sqrt{\left(\dfrac{\frac{K_R(V_{DD} - |V_{t,p}| - V_{t,n})}{L_n}}{(1+K_R)^2} * \Delta L_n\right)^2 + \left(\dfrac{\frac{K_R(V_{t,n} + |V_{t,p}| - V_{DD})}{L_p}}{(1+K_R)^2} * \Delta L_p\right)^2}$

(d) $\dfrac{\partial NM_L}{\partial W} * \Delta W = \sqrt{\left(\dfrac{\partial NM_L}{\partial W_n} * \Delta W_n\right)^2 + \left(\dfrac{\partial NM_L}{\partial W_p} * \Delta W_p\right)^2} = \sqrt{\left(\dfrac{\frac{K_R(V_{t,n} + |V_{t,p}| - V_{DD})}{W_n}}{(1+K_R)^2} * \Delta W_n\right)^2 + \left(\dfrac{\frac{K_R(V_{DD} - |V_{t,p}| - V_{t,n})}{W_p}}{(1+K_R)^2} * \Delta W_p\right)^2}$

Figure 7 shows that, for analytical model shown in (12), nominal value of NM_L decreases with the reduced supply voltage. For 0.8V supply voltage nominal value for noise margin (low state) is 406mV and for 1V of supply voltage noise margin increases up to 445mV. Noise margin is 425mV when V_{DD}=0.9V.

Unlike NM_H variation result, total NM_L variation due to process related issues, decreases as the supply voltage reduces. NM_L variation is lower than the NM_H variation. NM_L variation due to process related parameter variation decreases from 2.38% to 2.11% when V_{DD} reduces from 1V to 0.8V.

Table -4 illustrates the individual contribution of each parameter variation on overall NM_L variation. NM_L variation is more sensitive to supply voltage and threshold voltage variation. For V_{DD} =0.8V, VDD variation contribution is approximately 2.5X more than the effect of V_t variation. Like delay and NM_H variations, contributions of L and W variations are not significant. NM_L variation due to L and W variations decreases as supply voltage reduces. For V_{DD}= 0.8V, NM_L variations change in V_t is 0.76%. While change in L affects NM_L by 0.25%, change in W affects NM_L by 0.12% for the same supply voltage. To summarize V_{DD} variation remains the main dominant source for NM_L. For V_{DD} =0.8V, 5% variation in supply voltage can cause 1.95% variation in Noise Margin (Low State) of an inverter.
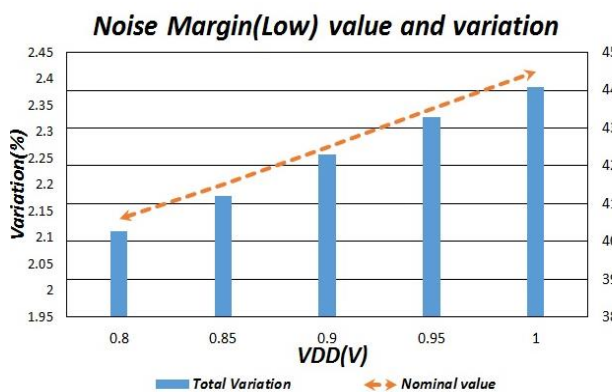

Fig.7 NM_L **variation versus supply voltage for an inverter in PTM's 22nm technology node**

Table -4 Noise Margin (Low State) variation

VDD(V)	VDD	Vt	L	W	Total	NM(mV)
	NM (Low) Variation (%)					
0.8	1.95	0.76	0.25	0.12	2.111	406
0.85	2.02	0.74	0.31	0.15	2.179	415
0.9	2.1	0.72	0.37	0.18	2.258	425
0.95	2.17	0.7	0.42	0.2	2.327	435
1	2.22	0.69	0.48	0.23	2.385	445

III. LOW VOLTAGE ANALOG CIRCUITS UNDER DEVICE VARIATIONS

Like digital circuits, the device variation map developed in Section I is also an important tool to understand the limitations and to make informed choices in analog circuits [2]. For example, one can make an informed decision of choosing the right bias current (Q-point) for an analog amplifier that meets the variability requirement by examining the load line drawn on the device variation map. Three Q-points in an analog amplifier has been shown in Figure 8. As shown Q-point 1 is located in the high-variation (red) region, where the device current variation is as high as 50%. Although Q-point 2 is desirable for maximum swing and dynamic range, a designer may not be comfortable in

choosing it, because it is in the orange region where there is over 35% of bias current variation. In this case, the designer may choose Q-point 3 in the green region, where the bias current is limited to about only 25%, even though leads to a lower dynamic range [2]. For analog circuits it is not beneficial to use short channel devices. Transconductance and gain of an analog circuit are dependent on the channel length of the transistor which are reduced in short channel device due to velocity saturation. In this paper, our analysis assumed long channel devices for analog circuits.
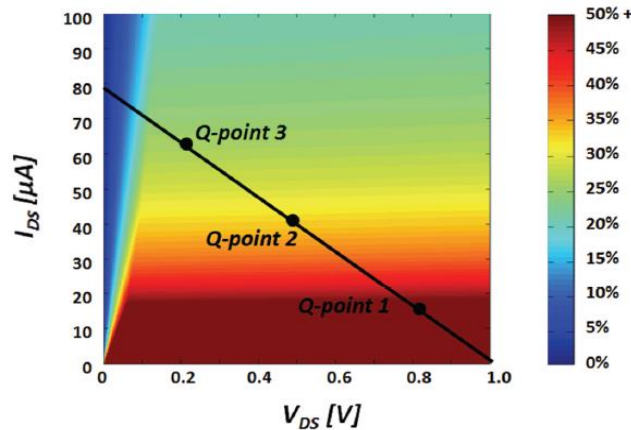

Fig. 8 The load line of an NMOS amplifier depicted on the device variation map using PTM's 22nm device parameters [2]

A. Current Source Variation

A similar technique of Section I has been used in this section to derive the variation on a current source transistor. This derived model is a useful tool to quantify the impact of device variation on analog circuits. Figure 9 demonstrates a current mirror, where Q_2 is used as a current source. The variation on I_{Out} can be derived by examining the drain-source current shown in figure 9[2].

Considering that the I_{DS} of Q_2 represent I_{out}, and Q_2 is only in saturation the variation of the output current can be derived as [2]:

$$\frac{\Delta I_{out}}{I_{out}} = \sqrt{\left(\frac{2\Delta V_{t,n}}{V_{OV}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2} \tag{13}$$

Where $V_{OV} = (V_{GS}-V_{t,n})$ is the overdrive voltage. The plot of device current variation component versus overdrive is illustrated in Figure 10. Device parameters for the 22nm technology node given in Table I and the analytical model in (13) has been used to generate this plot. From this figure we can see that, a very large output current variation occurs as the overdrive voltage is reduced. The analytical model provided in (13) also provides the contribution of each variability components, separately [2]. Figure 10 shows when device overdrive voltage is reduced below 400mV, threshold voltage variation is the dominant source of uncertainty. The impact of device parameter variation on output current uncertainty becomes unacceptable when the overdrive voltage is chosen to be very small. According to closed form model simulation, the impact of channel length and device width variations are negligible on bias current uncertainty in analog circuits. Analytical model's simulation suggested that the variation range will be in between 5.6% to 10.3% for an overdrive voltage ranging from 600 mV to 300mV. Effects of L and W variations are fixed at 2.5% and 1.2% respectively for different overdrive voltages. A 4% variation on V_t during processing can change the current of a current mirror by 9.87% when the circuit is biased at a overdrive voltage of 300mV.
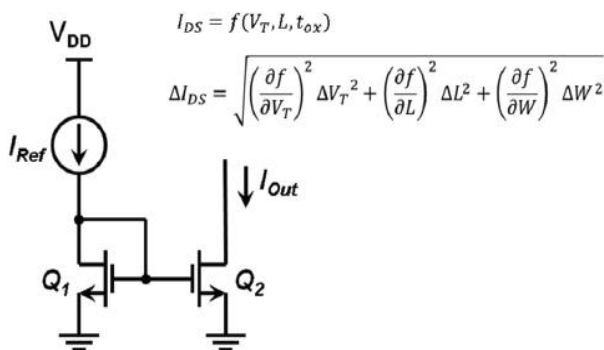

Fig. 9 Circuit diagram of a current source using current mirror configuration and related output current equation [2]
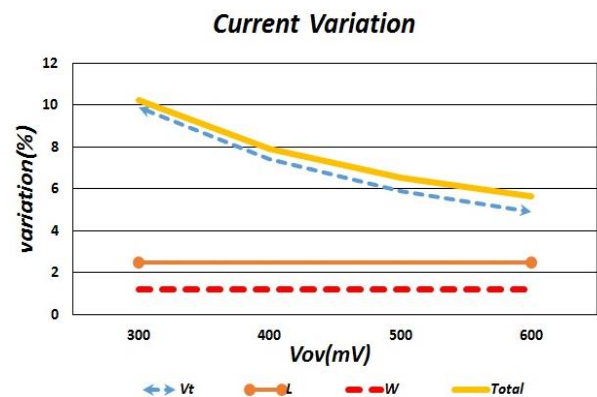

Fig. 10 The output current variation of a current source implemented in the PTM's 22nm technology node [2]

B. Gain Variation of a Differential Op-Amp

Furthermore, to analyze the effect of device variation in analog circuits we chose a Differential Pair Operational Amplifier (Op-Amp). In this section, we present effects on gain variation due to change in circuit parameters as described before (i.e. threshold voltage, effective channel length, and device width). Figure 11 shows a differential pair Op-Amp. Consider transistors in saturation region:

$$\text{Gain, } A_d = g_m (r_{o,n}\|r_{o,p}) = \frac{V_A'L}{(V_{GS}-V_{t,n})} \tag{14}$$

Where, $V_{OV} = (V_{GS}-V_{t,n})$ is the overdrive voltage. Taking partial derivatives and assuming that the variation of the device parameters is small compare to their nominal values and they can be approximated by Gaussian distribution, the device gain variation can be derived by taking the partial derivative.

$$\frac{\Delta A_d}{A_d} = \sqrt{\left(\frac{\Delta V_{t,n}}{V_{OV}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2} \tag{15}$$
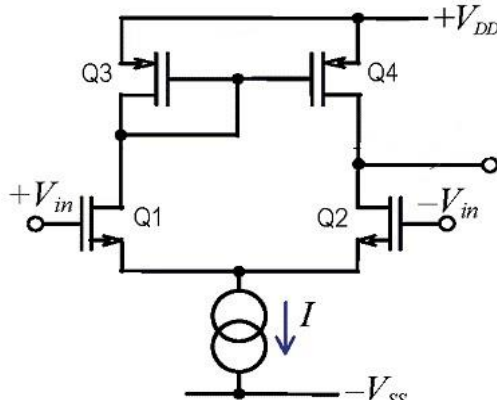

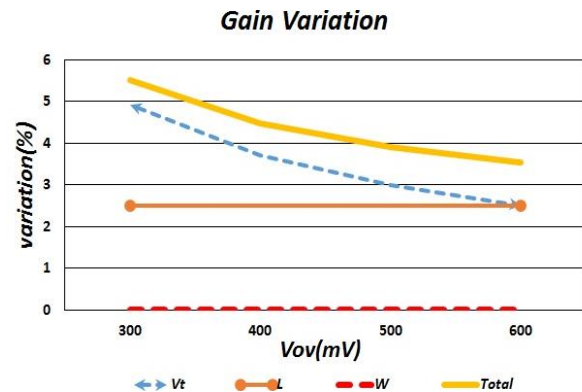Fig.11 Circuit diagram of a Differential Mode Op-Amp [11]

Fig.12 Gain variation versus overdrive voltage for a Differential Op-Amp in PTM's 22nm technology node

Figure 12 illustrates the effect of device parameter variations on a differential op-amp's gain for the analytical model of (15). Total variation on gain decreases as the as the V_{OV} increases. Again the V_t variation is the main parameter issue for gain variation in an Op-Amp circuit. Change in device width W has no effect in overall gain variation of a differential Op-Amp. While the effect of L variation is constant at 2.5% for any overdrive voltage. For 300mV overdrive voltage the total gain variation is around 5.5% and 3.5% for 600mV overdrive voltage.

CONCLUSION

A technique using partial derivative is presented in this paper to derive an analytical model for variability. Various analytical models for device variability are developed by using this technique. Both the analog and the digital circuits are analyzed by these models. These analytical models are applied on a 22nm CMOS process technology from the predictive technology model (PTM). Most of the results found from analytical models simulations are satisfactory and supports the theoretical assumptions. NM_H and t_{pHL} variations need more attention during the design since analytical simulation results show that they have dominant effect than NM_L when the supply voltage becomes very low. From analytical simulations, NM_L can vary up to 2.38%, whereas NM_H can vary as high as 8.7% (almost 4X higher than NM_L). However, NM_H is higher than NM_L for supply voltage is in between 1V and 0.9V range. For example, with 1V supply voltage, NM_L and NM_H are 445mV and 555mV respectively. Variations in analog circuits are found to decrease monotonously as the overdrive voltage increases from 300 mV to 600 mV. These process variations introduce vast area for research and these models are very effective tools in designing and making crucial decisions for low voltage analog and digital circuits operating in the super-threshold region. It is worth noting that there are several parameters other than threshold voltage, length and width that are not considered in the proposed analytical model. This work can be extended further to verify analytically the effects of other parameters in design variation of low voltage mixed signal circuits.

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