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Current-Mode DVCCCTA based KHN Filter with Two Capacitors and Two NMOS-Resistors

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ABSTRACT

A current-mode Kerwin-Huelsman-Newcomb (KHN) filter circuit based on differential voltage current-controlled conveyor transconductance amplifier (DVCCCTA) is presented. Second order low pass, high pass and band pass functions are realized. In the proposed circuit, three DVCCCTAs along with two NMOS-resistors and two capacitors are used. 0.25µm TSMC technology parameters are used. PSPICE software package is used in the simulation work.

Keywords: Current-mode, KHN, DVCCCTA, PSPICE

INTRODUCTION

Inductor and resistor are two important passive components in electronic circuits. Direct fabrication of these components on monolithic integrated circuits is difficult. Inductors are bulky in size. Large value of resistor is also problematic. So there is a need of circuits which not only perform desired functions but they did not need external passive components like inductors and resistors. This goal can be achieved using active devices. For instance, simulated inductors [1-9] are realized by the use of current conveyors. The current conveyors are active devices.

A circuit can be realized either in voltage-mode [10-12] or current [12-14]. Voltage-mode circuits are associated with some limitations. One of the major limitations is the gain-bandwidth product is constant. More bandwidth means less gain and vice versa. Limited slew rate, restricted dynamic range, inoperability on reduced power supply and high power consumption are some of the other limitations. On the other hand, current-mode circuits have several advantages over voltage-mode. One of the major advantages is the gain-bandwidth product is not constant. We can increase bandwidth without much sacrifice of gain. High slew rate, wide dynamic range and low power consumption are some of the other advantages of current-mode circuits. Current-mode circuits are realized using current conveyors. Current conveyors are considered as current-mode building blocks. So far many current conveyors are reported in the literature. DCCII (differential current conveyor), DVCCTA (differential voltage current conveyor transconductance amplifier), DVCCCTA (differential voltage current-controlled conveyor transconductance amplifier), CBTA (current backward transconductance amplifier), CDTA (current differencing transconductance amplifier), DDCCTA (differential difference current conveyor transconductance amplifier) and DVCC (differential voltage current conveyor) are some of the current conveyors [1, 3-5, 13 and 15-16].

DVCCCTA is a versatile and an important member in the family of current conveyors. Many analogue signal processing circuits are realized using current conveyors. Filters [14-17] are important analogue signal processing circuits. There are a large number of filter circuits in the literature. One of the famous filter is KHN (Kerwin-Huelsman-Newcomb) [15-16]. It is a biquad circuit. In this work, a current-mode KHN multifunctional filter is proposed using DVCCCTA. The proposed circuit has electronically tunability. We can control the bias current and change the intrinsic resistance of the circuit. The KHN circuit in [16] has digitally control variations but it has grounded passive resistors.

In the proposed circuit, there is no passive resistor. The proposed circuit has intrinsic resistances and NMOS-resistors. In this regard the proposed circuit is advantageous.

CIRCUIT DESCRIPTION

Block diagram of DVCCCTA is shown in Fig. 1. The CMOS implementation of DVCCCTA is shown in Fig. 2.

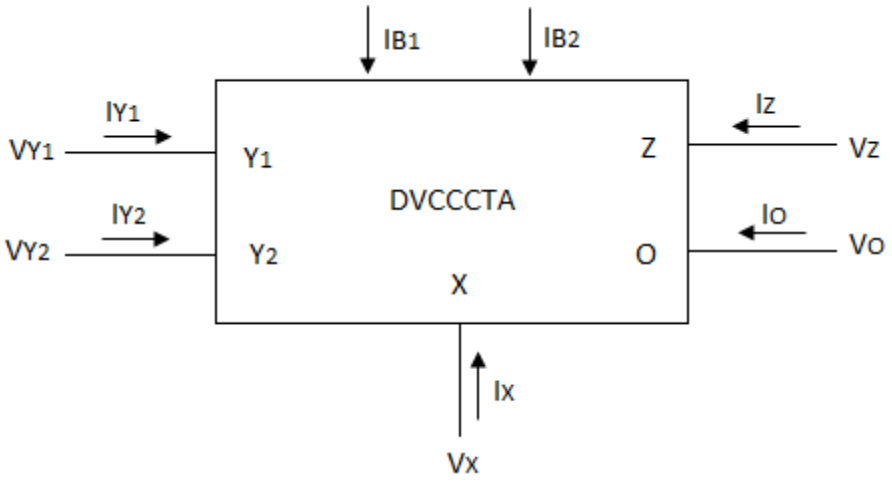

Fig.1 Block diagram of DVCCCTA [4]

The characteristics of DVCCCTA in the matrix representation are given below.

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & R_X & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & g_m & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \\ V_O \end{bmatrix}$$

In the above matrix R_X is the intrinsic resistance at node X and g_m is the transconductance from node Z to node O. R_X depends on I_{B1} and gm is controlled by I_{B2}.

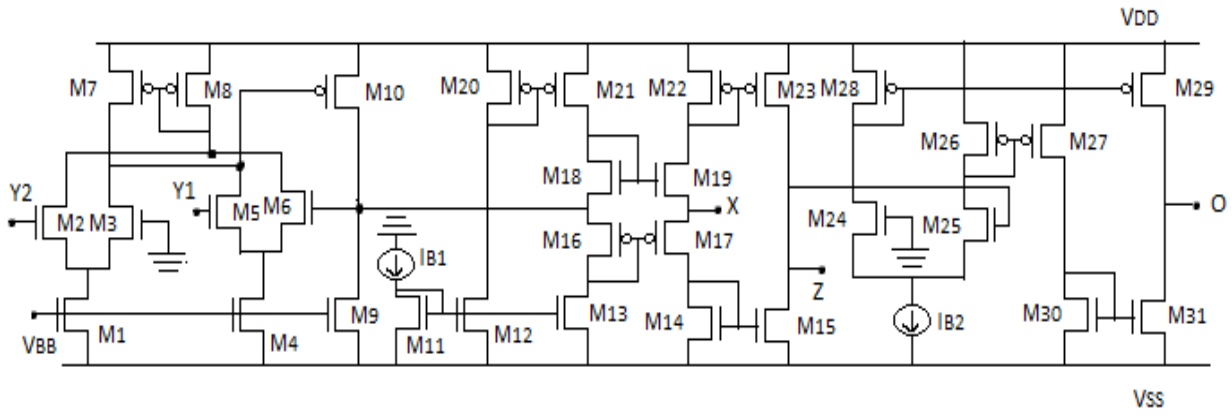

Fig.2 A CMOS model of DVCCCTA of Fig. 1 [4]

Table-1 The Aspect Ratios of Various Transistors of fig.2 as used in the simulation work

Aspect ratio (W(μm)/L(μm))	Transistors
3/0.25	M_1, M_4, M_{11}- M_{15}, M_{30}- M_{31}
1/0.25	M_2, M_3, M_5, M_6, M_9
5/0.25	M_7 -M_8, M_{20}- M_{23}, M_{26}, M_{28}- M_{29}
12.5/0.25	M_{10}
8/0.25	M_{16}-M_{17}
5/0.25	M_{18}, M_{19}
5/0.25	M_{24}-M_{25}
4.35/0.25	M_{27}

The proposed current-mode KHN is shown in Fig. 3.

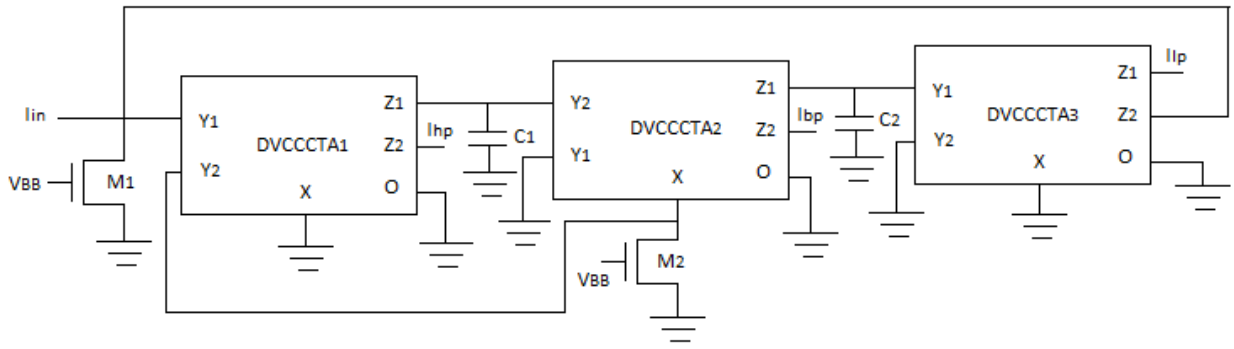

Fig. 3 Proposed current-mode KHN

The circuit in Fig. 3 is simulated in PSPICE. 0.25µm TSMC CMOS technology parameters are used. NMOS transistors M_1 and M_2 are used as resistors. When a MOS transistor operates in the triode region, it can be used as resistor ($V_{DS} < (V_{GS}-V_t)$). An additional Z-terminal is used in the DVCCCTA to obtain the required responses.

Analysis of circuit in Fig. 3 gives the following equations.

$$\frac{Ilp}{Iin} = \frac{\frac{R1}{C1C2(Rx2+R2)Rx1Rx3}}{S^2 + \left(\frac{R2}{C1(Rx2+R2)Rx1}\right)S + \frac{R1}{C1C2(Rx2+R2)Rx1Rx3}} \tag{1}$$

$$\frac{Ihp}{Iin} = \frac{S^2\frac{R1R2}{Rx1Rx3}}{S^2 + \left(\frac{R2}{C1(Rx2+R3)Rx1}\right)S + \frac{R1}{C1C2(Rx2+R2)Rx1Rx3}} \tag{2}$$

$$\frac{Ibp}{Iin} = \frac{S\frac{R1}{C1Rx1(Rx2+R2)}}{S^2 + \left(\frac{R2}{C1(Rx2+R2)Rx1}\right)S + \frac{R1}{C1C2(Rx2+R2)Rx1Rx3}} \tag{3}$$

Eq. (1), Eq. (2), and Eq. (3) represent low pass filter, high pass filter and band pass filter respectively. In these equations, R_1 and R_2 are the resistances of the NMOS transistors M_1 and M_2 respectively. R_{x1}, R_{x2} and R_{x3} are the intrinsic resistances of the DVCCCTA1, DVCCCTA2 and DVCCCTA3 respectively.

SIMULATION WORK, RESULTS AND DISCUSSION

The proposed filter is simulated using .25µm TSMC model parameters. One more Z-node has been added to the CMOS DVCCCTA circuit of Fig. 2. The circuit of Fig. 2 with an additional Z-node is used in the circuit of Fig. 3. The supply voltages are taken as V_{DD}= -V_{SS}= 1.25V, V_{BB}=0.8V. The bias current is selected as I_{B1}= 10µA and I_{B2}= 160µA.For M1(which represent R_1), W=1.5µ, L=.25 µ and for M_2(which represent R_2), W=1.25 µ, L=.25 µ. The input current, I_{in}= 1 µA. Fig. 4(a) shows low-pass, high-pass and band-pass responses when C_1= C_2 =100pF. The simulated frequency (3-dB cutoff) is found to be 601.56KHz for low pass function. The result presented in Fig. 4(b) when C_1=C_2=50pf. The simulated frequency (3-dB cutoff) is found to be 1.20MHz for low pass filter. The result presented in Fig. 4(c) when C_1=C_2=10pf. The simulated frequency (3-dB cutoff) is found to be 5.97MHz for low pass filter. The parameters used for simulation are listed in appendix.

Appendix

0.25µm TSMC CMOS technology parameters are listed below.

MODEL NAME NMOS (LEVEL = 3 TOX = 5.7E-9 NSUB=1E17 GAMMA= 0.4317311 PHI = 0.7 +VTO = 0.4238252 DELTA=0 UO= 425.6466519 ETA =0 THETA = 0.1754054 KP = 2.501048E-4 +VMAX = 8.287851E4 KAPPA= 0.1686779 RSH= 4.062439E-3 NFS= 1E12 TPG =1 XJ = 3E-7 +LD=3.162278E-11 WD = 1.232881E-8 CGDO = 6.2E-10 CGSO = 6.2E-10 CGBO=1E-10 CJ = 1.81211E-3 +PB = 0.5 MJ = 0.3282553 CJSW = 5.341337E-10 MJSW = 0.5)

MODEL NAME PMOS (LEVEL = 3 TOX= 5.7E-9 NSUB = 1E17 GAMMA = 0.6348369 PHI = 0.7 +VTO= -0.5536085 DELTA = 0 UO = 250 ETA= 0 THETA= 0.1573195 KP = 5.194153E-5 +VMAX = 2.295325E5 KAPPA = 0.7448494 RSH = 30.0776952 NFS= 1E12 TPG = -1 XJ = 2E-7 +LD = 9.968346E-13 WD = 5.475113E-9 CGDO= 6.66E-10 CGSO = 6.66E-10 CGBO = 1E-10 +CJ = 1.893569E-3 PB= 0.9906013 MJ= 0.4664287 CJSW = 3.625544E-10 MJSW = 0.5)

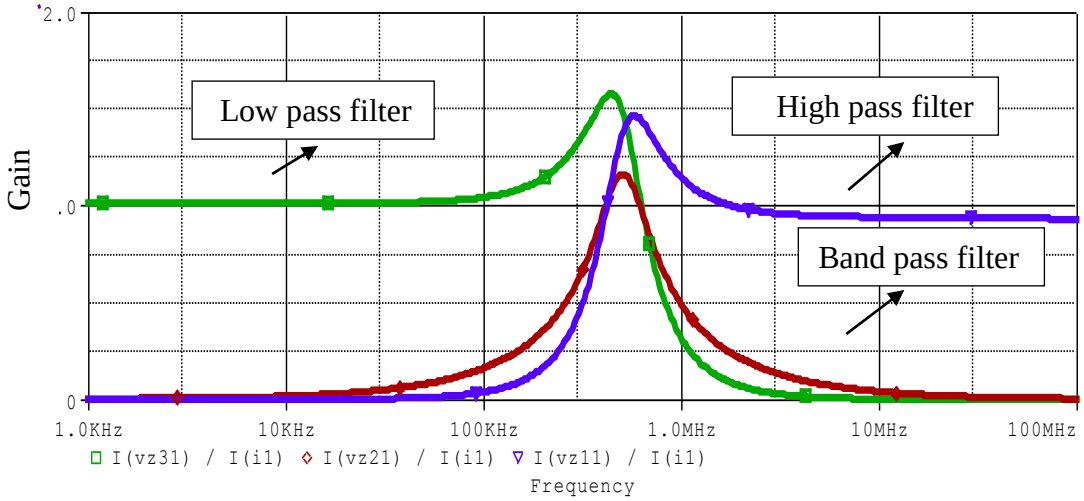

Fig. 4(a) Simulation result of KHN filter [3-dB cutoff of low pass filter is 601.56KHz, 3-dB cutoff of high pass filter is 427.51KHz and 3-dB bandwidth of band pass filter is 345.71KHz]

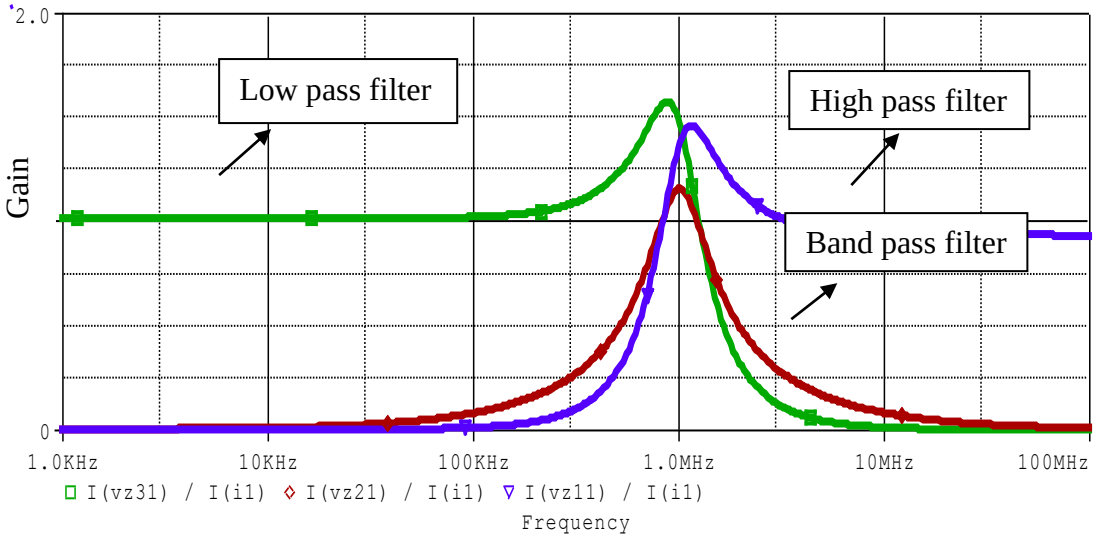

Fig. 4(b) Simulation result of KHN filter [3-dB cutoff of low pass filter is 1.20MHz, 3-dB cutoff of high pass filter is 854.14KHz and 3-dB bandwidth of band pass filter is 694.12KHz]

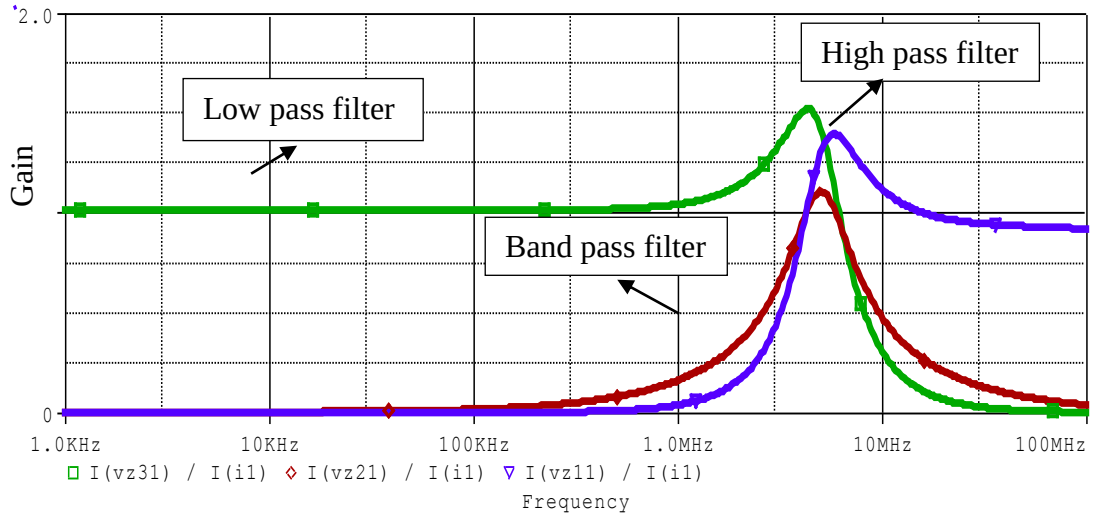

Fig. 4(c) Simulation result of KHN filter [3-dB cutoff of low pass filter is 5.97MHz, 3-dB cutoff of high pass filter is 4.24MHz and 3-dB bandwidth of band pass filter is 3.58MHz]

It is clear from simulation results that the filter works in the range of KHz to several MHz. From Fig 4(a) and Fig. 4(c) it is clear as, that when capacitance values go down by a factor of 10, the 3-dB cutoff frequency increases by a factor approximately equal to 10.

CONCLUSION

A current-mode DVCCCTA based KHN filter is presented. Three DVCCCTAs along with two capacitors and two NMOS-resistors were used in the simulation. The filter circuit is simulated in PSPICE using 0.25µm TSMC CMOS technology parameters. The filter works in the range of KHz to several MHz. Moreover, the circuit is electronically tunable. Since the circuit has active components and capacitors, it can easily be fabricated on monolithic integrated circuit.

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