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Comparative Analysis of Vedic and Array Multiplier

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ABSTRACT

Most of the today's real time signal processing algorithm include multiplication as its processing heart. It is most important arithmetic unit in Microprocessor & DSPs. The speed & power consumption & packaging of the processor is mainly determined by its multiplier. Two important parameters associated with multiplication performed in Processors applications are latency and throughput. Latency is the 'real delay of computing a function'. Throughput is a measure of 'how many computations can be performed in a given period of time'. The execution time ofmost processor is dependent on its multipliers, and hence need for high speed multiplier arises. The objective of this manuscript is to simulate and compare both Vedic & Array multiplier for different bit lengths i.e. two, four, eight & sixteen bit on Model Sim-Altera 6.6d (Quartus II 11.0sp1) Starter Edition using VHDL language and then implementation them on Xilinx 14.4 with family Spartan6, device as XC6SLX45, package CSG324 with speed grade of -3 for comparative analysis.

Keywords: Array, Vedic multipliers, Urdhvatiryakbhyam sutra, LUTs, Fan Out, Delay

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INTRODUCTION

Multiplication is most useful arithmetic operation and widely used in Microprocessors, DSP and other Communication applications. Most of the DSP algorithms require real-time processing with several multiplications. Multiplication is the steps of adding a number of partial products. Multiplication algorithms differ in terms of partial product generation and partial product addition to produce the final result. A normal multiplier block consists of a sequence of AND gates to generate the partial product terms and used adders to add them. For higher order multiplications, a huge number of adders are used to perform the addition of partial product. The speed limitation is largely associated with conventional multiplier architectures due to the latency introduced by number of adder structures. For high speed processors requirement, the need of high speed multiplier is increased. An efficient multiplier unit is designed in term of low power consumption, high speed, low area, minimum delay. The conventional mathematical algorithms can be simplified and optimized by the use of Vedic mathematics [1]. By using this technique, we can increase the computational speed of processor to perform fast arithmetic operations. Vedic multiplier (VM) is the fastest multiplier and it is based on Vedic multiplication formula called sutra. The main advantage of Vedic Multiplier is that the generation of partial product and their addition are done concurrently. Vedic techniques reduce the complexity, execution time of the system, power, area etc.

ARRAY MULTIPLIER

Array multiplier is a proficient layout of a combinational multiplier. Multiplier circuit is based on add and shift algorithm. Every partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product is shifted according to their bit orders and then added [2-3]. Multiplication of two binary numbers can be obtained by using AND logic gate that produced the product bit. The various product terms generated by an array of AND gates are given to the Adder array.

In array multiplier, let us consider two binary numbers A and B, of m and n bits, being the multiplicand and multiplier respectively. The mn summands are produced in parallel by a set of mn AND gates. Here, n x n multiplier requires n (n-2) full adders, n half-adders and n2 AND gates. Also, in array multiplier worst case delay would be (2n+1) td. To simplify the concept, for 2X2 bit multiplication, assuming A = a(1)a(0) and B= b(1)b(0), the various bits of the final product term P can be written as:-

$$P(0) = a(0)b(0)$$
$$P(1) = a(1)b(0) + b(1)a(0)$$
$$P(2) = a(1)b(1) + C1;$$

where C1 is the carry generated during the addition for the P(1) term.
P(3)=C2; where C2 is the carry generated during the addition for the P(2) term.

For the above multiplication, an array of four AND gates is required for the various product terms like a(0)b(0) etc. and an Adder array is required to find the sums involving the various product terms and carry combinations mentioned in the above equations in order to obtain the final Product bits.

In fig.1, describes the 4x4 multiplication process using array multiplication method, say A= A3 A2 A1 A0 and B= B3 B2 B1 B0. The output line for this multiplication is P7 P6 P5 P4 P3 P2 P1 P0.

Array Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger [4]. It also requires larger number of gates because of which area is also amplified; due to this array multiplier is less economical. Thus, it is a fast multiplier but hardware complexity is high [5-6].

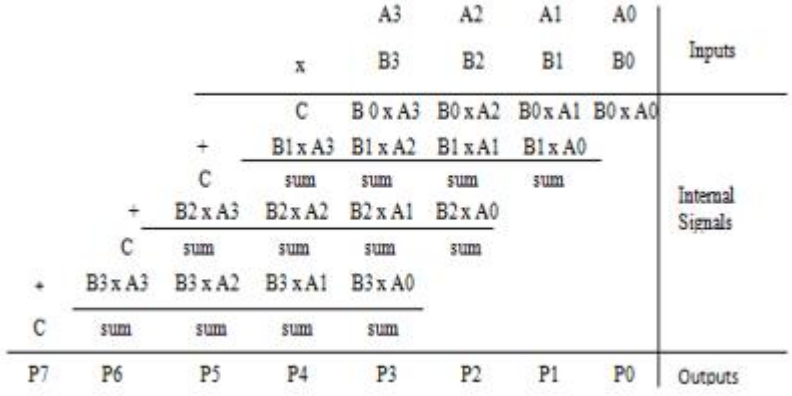

Fig.1 Four-bit Array Multiplier

VEDIC MULTIPLIER

The Vedic mathematics is the very old system of mathematics which has an inimitable technique for fast calculations, based on 16 sutras. Vedic mathematics is part of four Vedas (books of wisdom). It is ingredient of Sthapatya-Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, trigonometry, geometry (plane, co-ordinate), quadratic equations, factorization and even calculus. It was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas) by Tirtha (1884-1960). Vedic Mathematics offers a simple and highly efficient approach to mathematics. The brilliance of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics. It is not only a mathematical wonder but also it is logical. That's why Vedic Mathematics has such a degree of eminence which cannot be disapproved. Due to these phenomena, Vedic Mathematics has already crossed the boundaries of India and has become a leading topic of research abroad. Vedic Mathematics deals with numerous basic as well as complex mathematical operations [7,9].

URDHVA TIRYAKBHYAM SUTRA

The multiplier is based on an algorithm UrdhvaTiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. 'Urdhva' and 'Tiryagbhyam' words are derivative from Sanskrit literature. Urdhva means 'Vertically' and Tiryagbhyam means 'crosswise' [8]. It is based on a novel concept, where the generation of all partial products can be done with the concurrent addition of partial product UrdhvaTiryakbhyam Sutra is a general multiplication formula valid to all cases of multiplication. Anyone can easily realize that this Vedic method probably makes difference for mental calculations. If somebody tries to do multiplication mentally, in a conventional method, one would have to remember first row, then second row and likewise; then add all of them [10-12].

The digits on the two ends of the line are multiplied and the product is added with the previous carry. When there are extra lines in one step, all the results are added to the previous carry. The least significant digit of the number so obtained acts as one of the result digits and the rest act as the carry for the next step. Initially the carry bit is taken to be as zero. The line diagram for multiplication of two 4-bit numbers is as shown in fig. 2.

Multiplication methods that many of processors are using today has inspired by Vedic multiplier introduced in Indian Vedas with different 16 sutras. Vedic multiplier uses bit-wise multiplication with simultaneous product term finding and its column-wise addition. It is one of the best benchmark for fast multiplication algorithm [13,15].

The 8-bit Vedic Multiplier has been designed using four 4 bit Vedic Multipliers and three Ripple Carry Adders as well as Kogge Stone Adders each of 8 bit, 12 bit.The 16-bit Vedic Multiplier has been designed using four 8 bit Vedic Multipliers and three Ripple Carry Adders as well as Kogge Stone Adders each of 16 bit, 24 bit, 24 bit. It is found that as the number of bits increases in the multiplier the performance of the system increases [14].

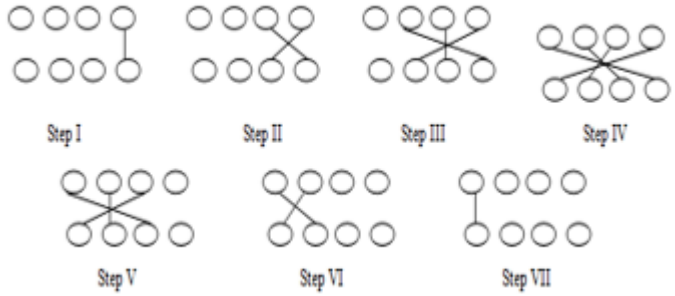

Fig. 2 Four Bit Vedic Multiplier

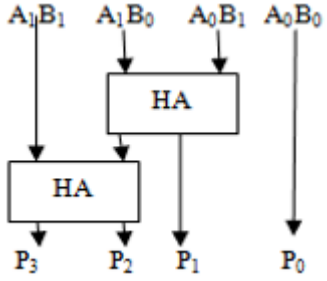

Fig.32x2 bit Vedic basic element

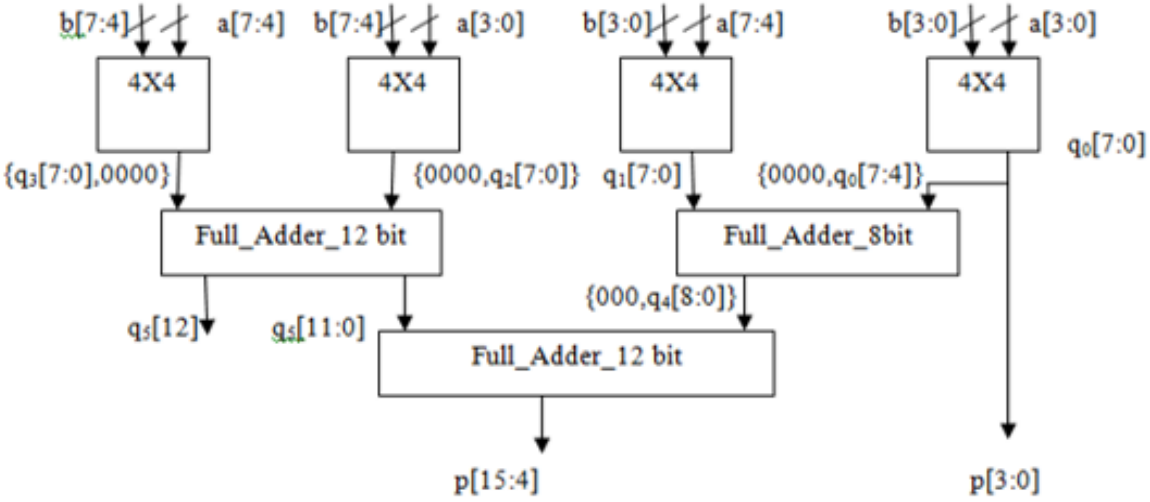

Fig.4 8x8 bit Vedic basic element

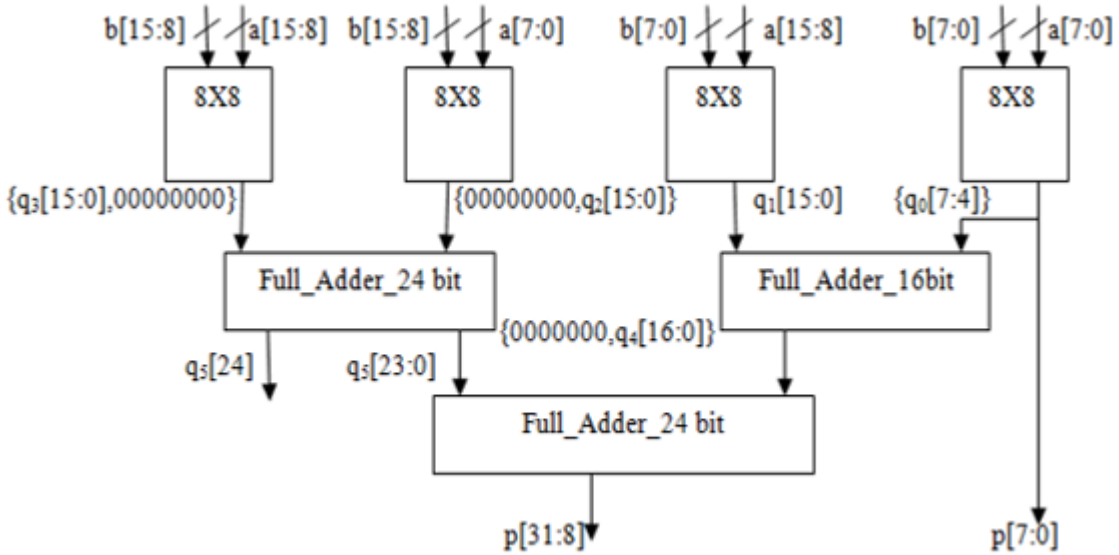

Fig.4 16x16 bit Vedic basic element

SYNTHESIS & SIMULATION

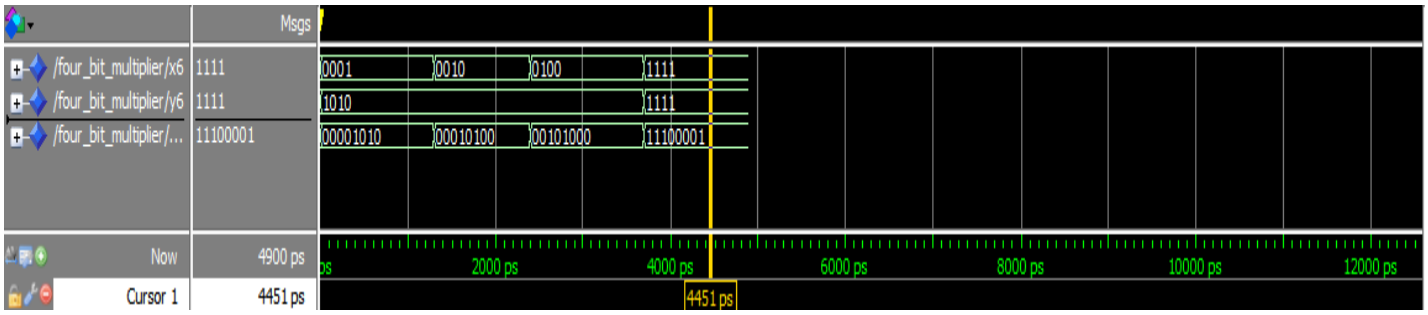

Fig. 5 Simulation Result of 2-bit Vedic Multiplier

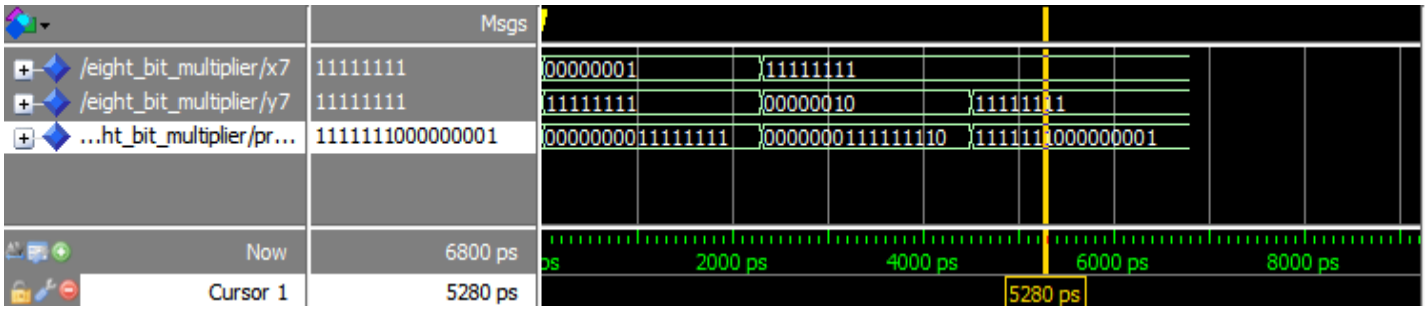

Fig. 6 Simulation Result of 4-bit Vedic Multiplier

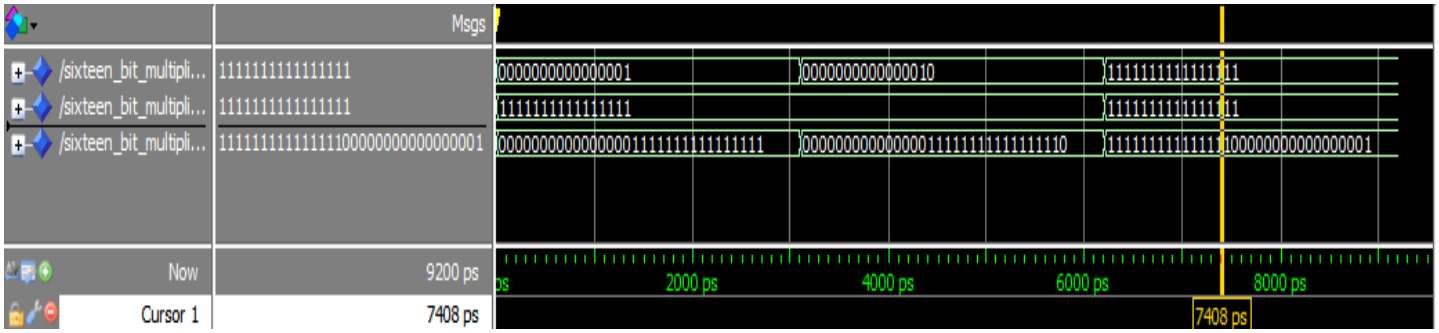

Fig. 7 Simulation Result of 8-bit Vedic Multiplier

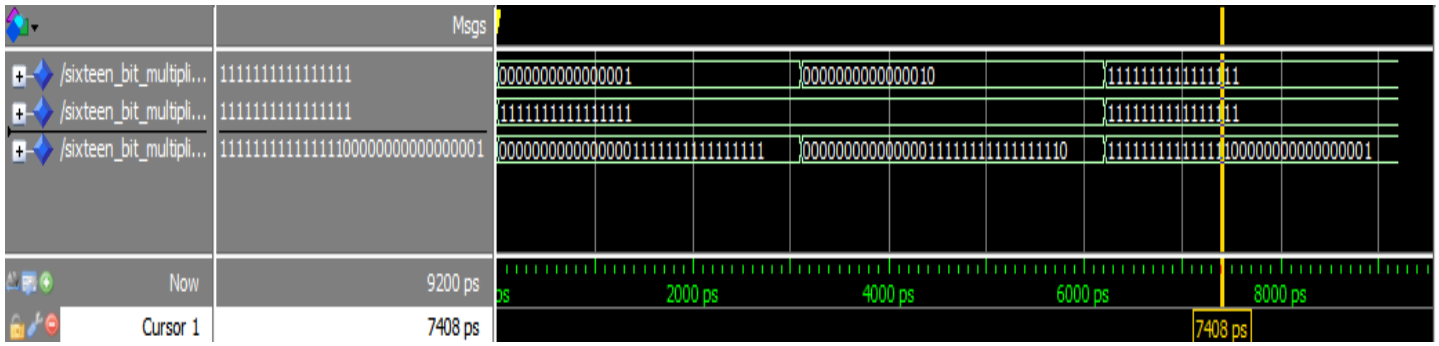

Fig. 8 Simulation Result of 16-bit Vedic Multiplier

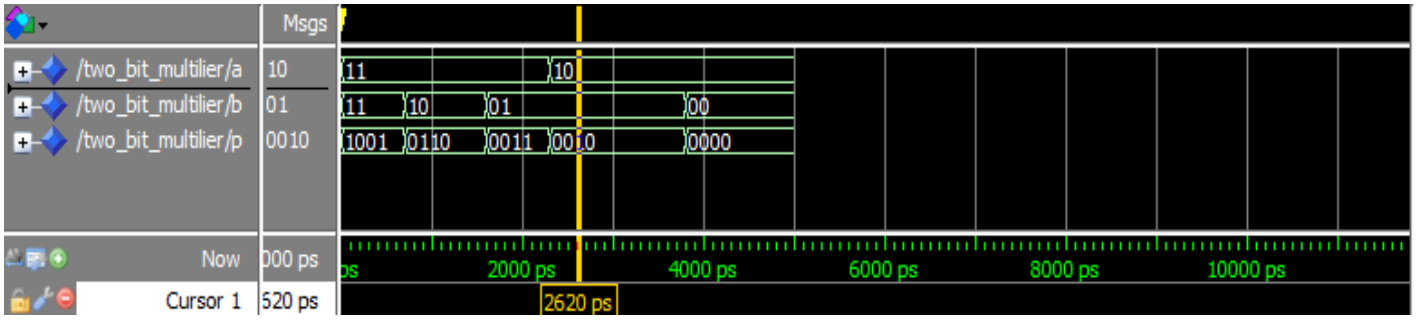

Fig. 9 Simulation Result of 2-bit Array Multiplier

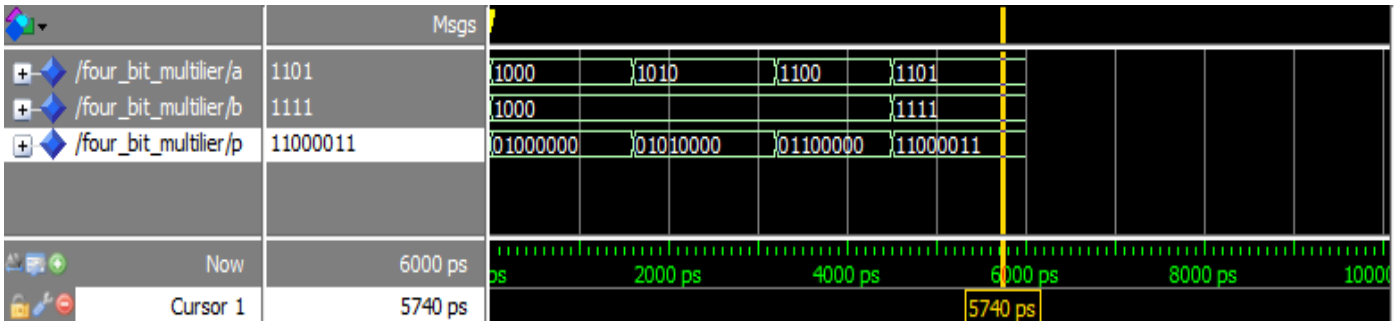

Fig. 10 Simulation Result of 4-bit Array Multiplier

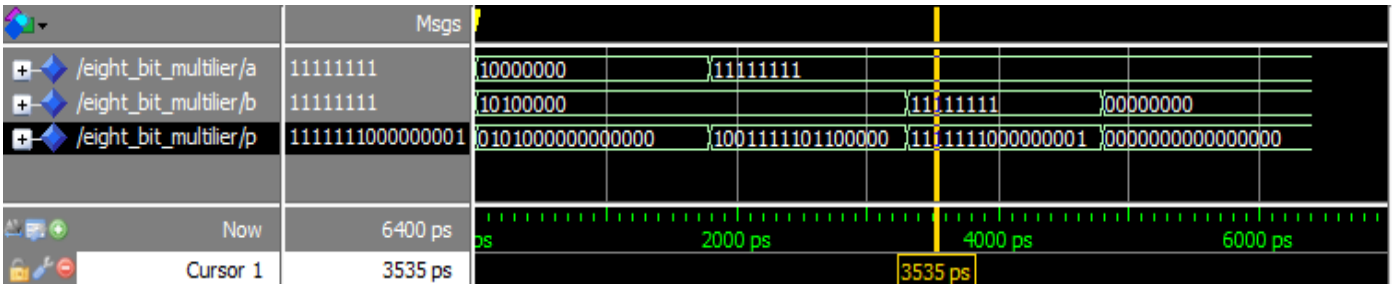

Fig. 11 Simulation Result of 8-bit Array Multiplier

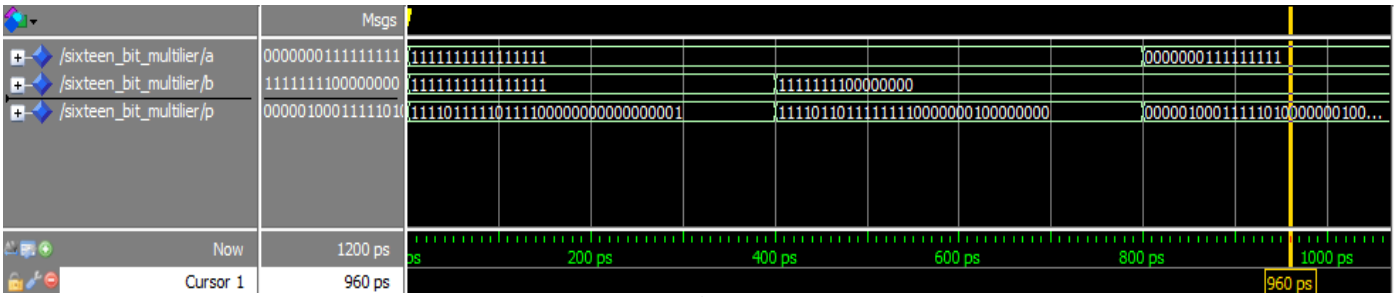

Fig. 12 Simulation Result of 16-bit Array Multiplier

IMPLEMENTATION

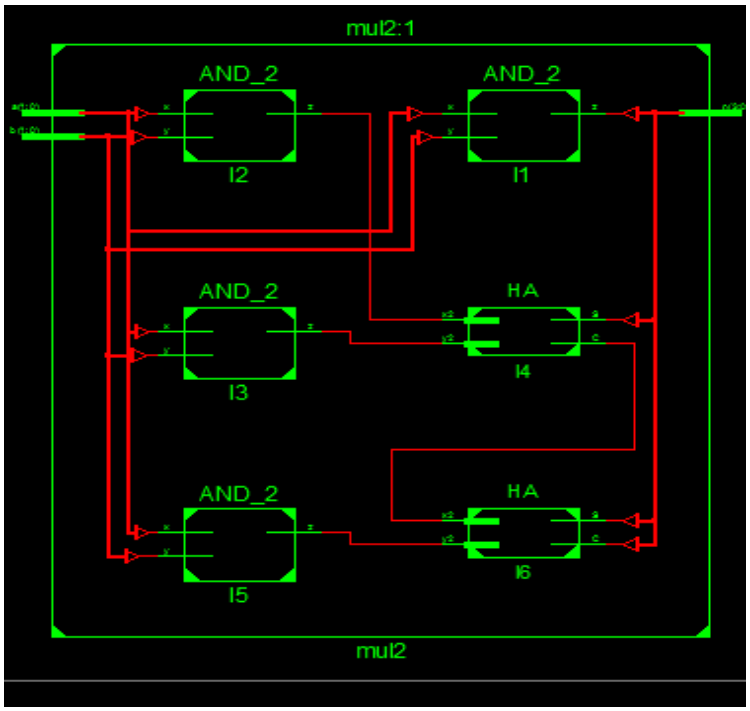

Fig.13 RTL Schematic for 2 bit Vedic multiplier

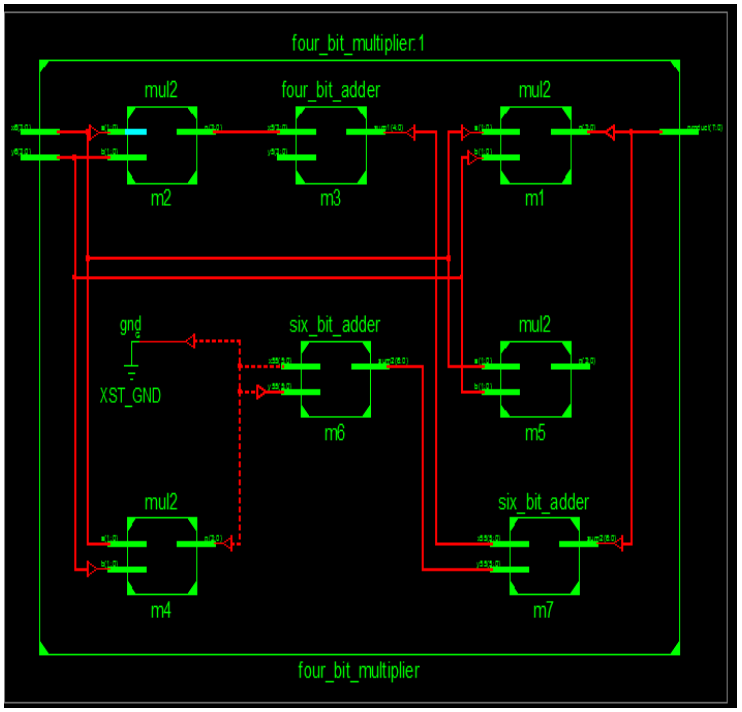

Fig.14 RTL Schematic for 4 bit Vedic multiplier

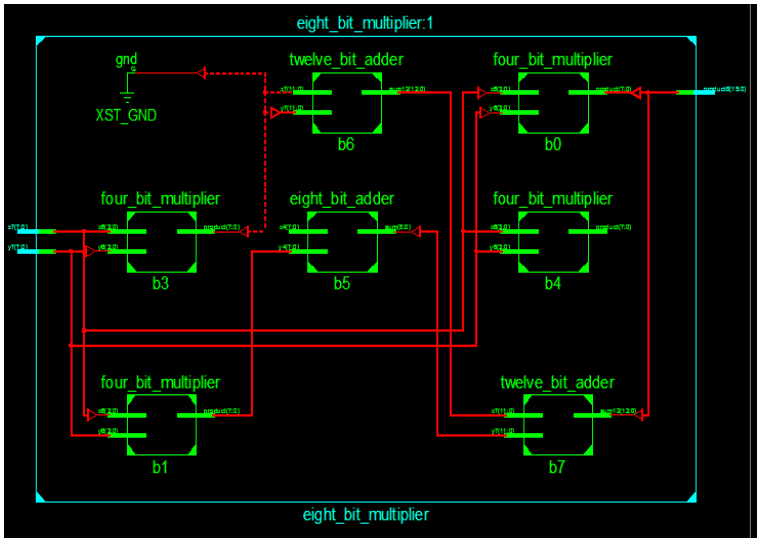

Fig.15 RTL Schematic for 8-bit Vedic multiplier

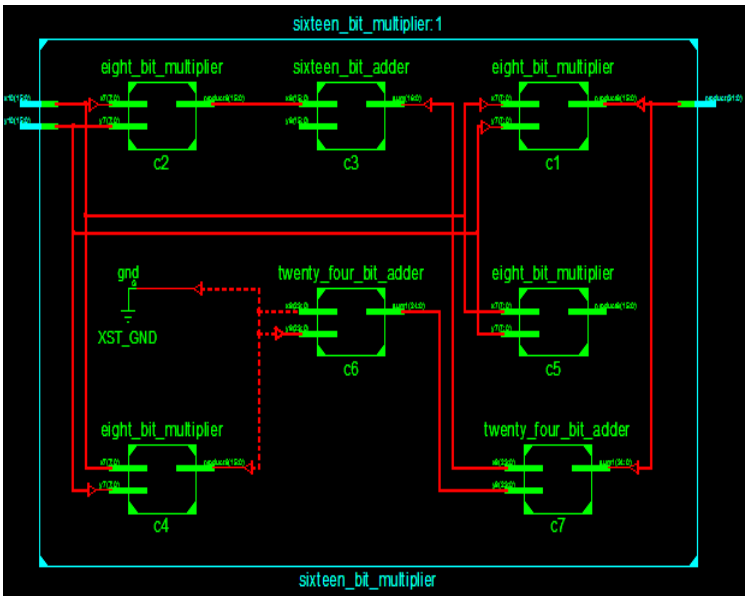

Fig.16 RTL Schematic for 16 bit Vedic multiplier

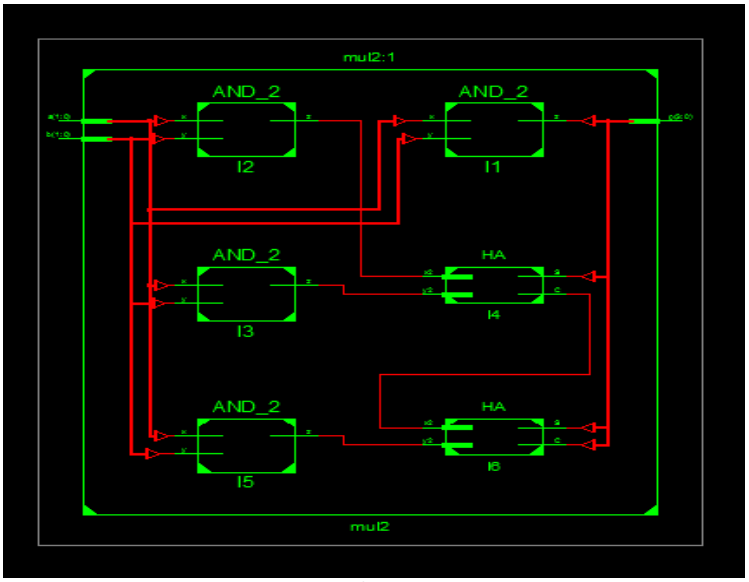

Fig.17 RTL Schematic for 2 bit Array multiplier

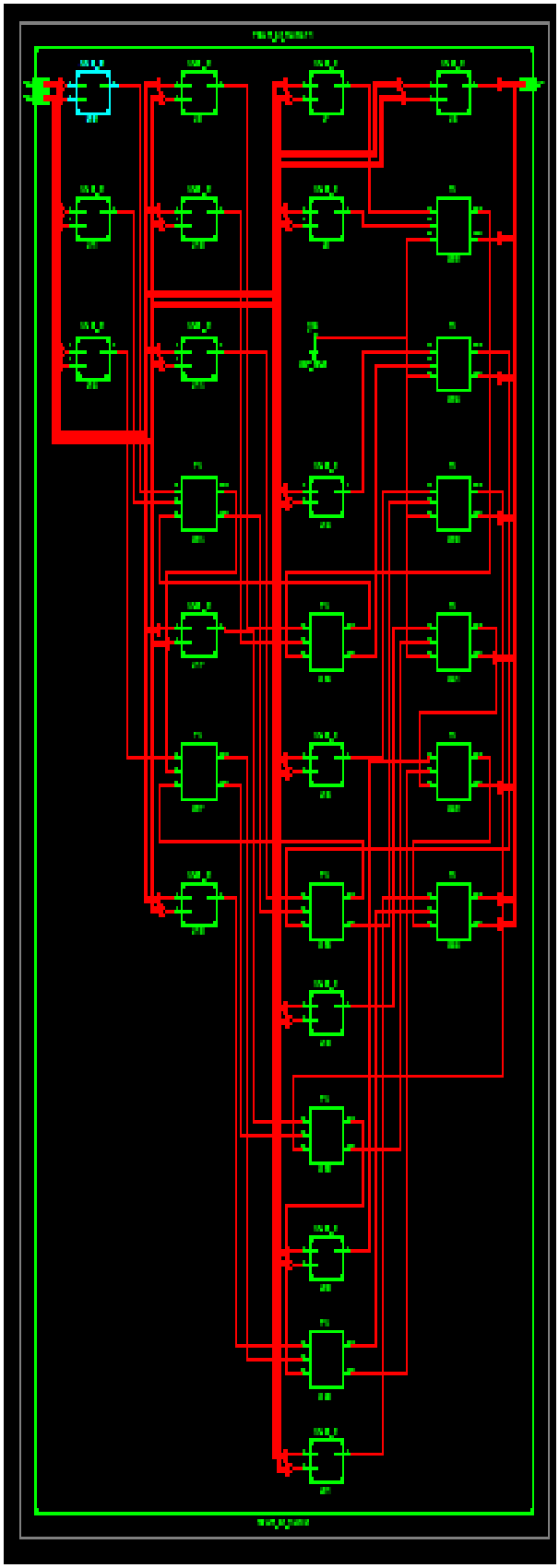

Fig.18 RTL Schematic for 4 bit Array multiplier

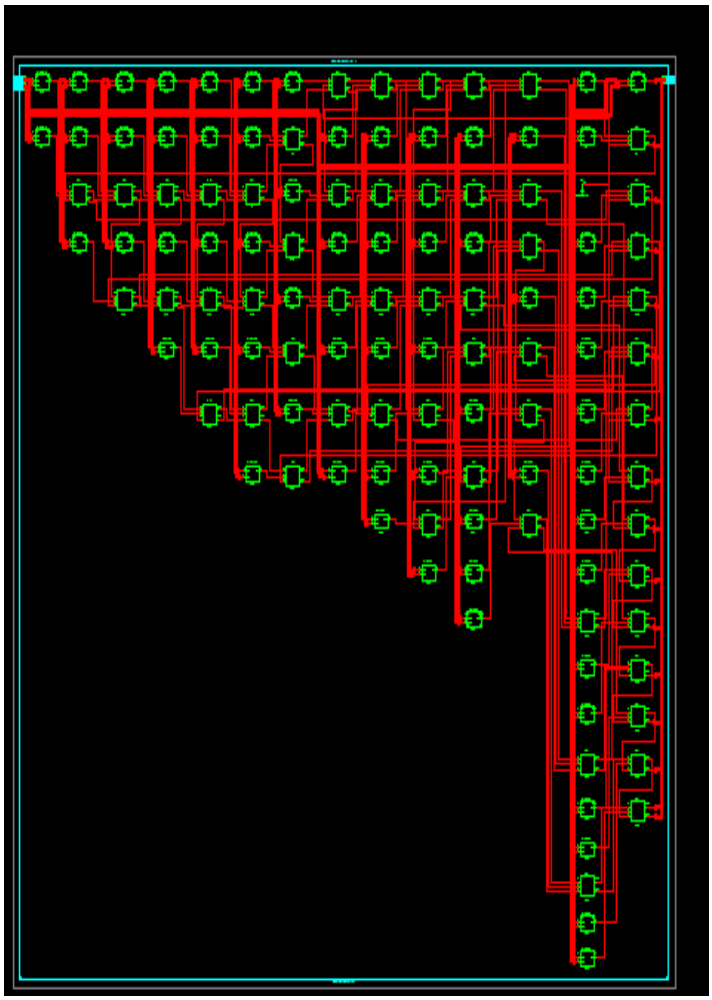

Fig.19 RTL Schematic for 8-bitArray multiplier

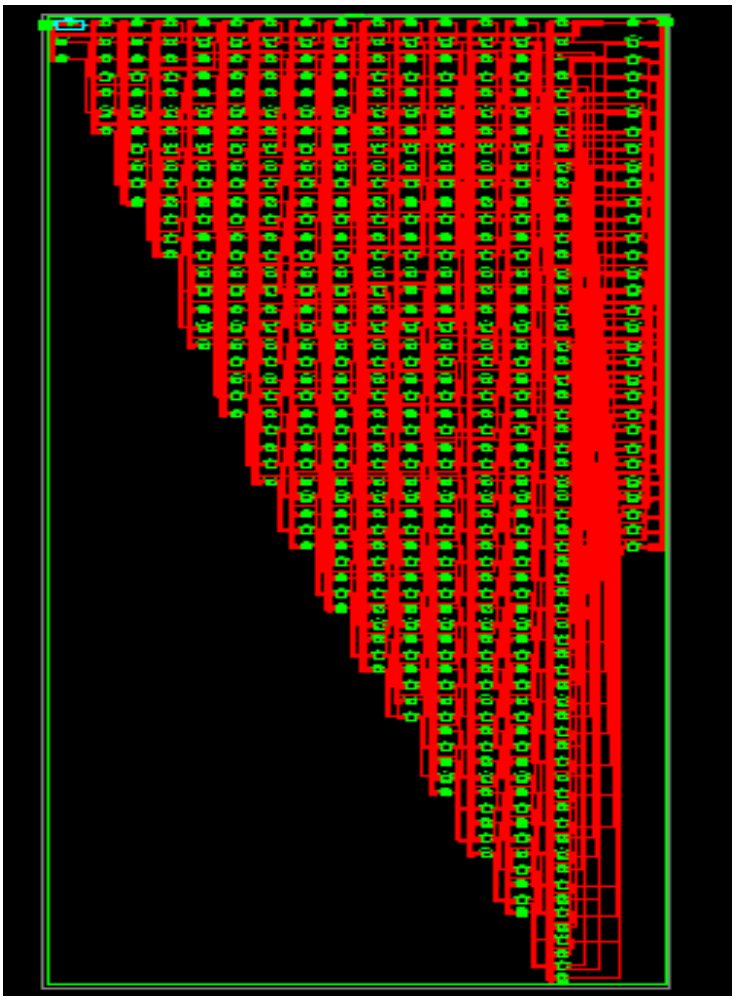

Fig.20 RTL Schematic for 16-bitArray multiplier

COMPARATIVE ANALYSIS

Simulation has been done on Model-Sim Altera Edition 6.6d &Implementation has been done on Xilinx 14.4 with family Spartan6, device as xc6slx45, package csg324 with speed grade of -3. Synthesis report obtained for the above multiplier provides us many parameters such as Delay, Levels of Logic, Memory, No. of slice, no. of LUTs and many more for comparative analysis of vedic& Array multiplier for different bit-lengths.

Table -1 Comparison b/w Vedic & Array Multiplier for Different Bit Length on DeviceSpartan6 XC6SLX45-CSG324

Bit Length	Type	Delay(ns)	Levels of Logic	No. of slice LUTs	Memory (KB)
4	Vedic	7.942	5	7	255024
	Array	55.591	40	38	257284
8	Vedic	18.270	15	121	257988
	Array	120.485	175	82	259588
16	Vedic	27.278	23	656	259076
	Array	263.072	734	178	260868

CONCLUSION

From implementation, simulation & comparative results, it is concluded that delay in Array multiplier is nearly ten times the Vedic multiplier, a better choice for fast application Higher the no. of look-up tables in Array multiplier reducing its packaging density i.e. chips will have more accessing area. Also memory occupied by Array multiplier is relatively more than Vedic multiplier. Overall it can be said that the performance of Vedic multiplier is better than that of Array multiplier. By utilizing the findings of this manuscript, the analysis may be carried out for Wallace Tree and Shift & Add Multiplier. If work is carried out for higher bit configuration, then their will be clear distinction between different types of multiplier.

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