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Improved Two Phase Clocked Adiabatic Static CMOS Logic Circuit

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ABSTRACT

This paper proposes an improved Two Phase Clocked Adiabatic Static CMOS logic (2PASCL) circuit. The proposed circuit is based on energy recovery adiabatic principle which consumes less power. The number of transistor required in proposed circuit is same as that of reported 2PASCL. Various combination circuits such as inverter, NAND, NOR, XOR has been designed using both the logic style. A two phase complementary sinusoidal power clock has used with different frequency. Detailed power analysis, delay analysis, Power Delay product analysis between proposed 2PASCL, Reported 2PASCL and CMOS logic has been performed over a frequency range from 20Mhz to 100 Mhz. In the proposed inverter and combinations circuits the power efficiency has been improved to almost 18% compared to CMOS and reported 2PASCL logic. Also it has been observed that if input signal frequency is equal or doubled the clock frequency then the proposed circuit gives best performance. The 2PASCL technology finds application in low power digital devices.

Keywords: Adiabatic switching, low power, energy recovery, power clock

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INTRODUCTION

Due to wide diffusion of portable devices, power reduction has become key concern in design of low power circuits. The conventional complementary metal oxide semiconductor (CMOS) circuit dissipate energy while switching. In CMOS power dissipation is proportional to square of power supply voltage. Total energy dissipation is given by $E=C_LV_{dd}^2$ Therefore power dissipation can be achieved by reduction in supply voltage and switching activity [1-4]. A novel Adiabatic logic approach have been proposed for low power circuits [5]. This adiabatic logic is based on the energy recovery principle. it uses clocked ac voltage supply which acts as power clock to slowly charge the node capacitances and to reduce energy dissipation by recycling the energy stored in the nodes of circuits. [6-7]. several adiabatic logic circuits with different clocking scheme have been analysed over the past years for low power circuit applications [8-9].

In this paper, we considered two phase clocked adiabatic static CMOS logic (2PASCL) circuit [10-11] because of its lower switching activity. We presented improved structure for two phase clocked adiabatic static CMOS logic (2PASCL). It gives less power dissipation over the reported one. it utilizes two sinusoidal power clock. The height of each sinusoidal power clock is 1.8v. The two power clocks are 180^0 phase shifted with each other. This paper describes proposed and reported 2PASCL structure with the combination circuits such as NAND gate, NOR gate, OR gate and proposed logic style. The simulated results so obtain as proposed logic gives less power dissipation, the comparative power dissipation, delay analysis is summarized in the paper.

PROPOSED AND REPORTED 2PASCL CIRCUIT

Reported Two Phase Clocked Adiabatic Static CMOS Logic

Two phase clocked adiabatic static CMOS logic [10] utilizes the principle of adiabatic switching. It can be derived from CMOS circuits. The switching activity of 2PASCL is less than the dynamic logic. Fig. 1 shows the structure of 2PASCL.The transistor P1 and N1 are recycling the charges from the output and if the signal nodes are preceded by long chain then the P1 and N1 are improving discharging speed of intermediate nodes. The circuit uses two sinusoi-

dal power clock which are 180^0 phase shifted to each other. Fig 2 shows waveform of 2PASCL inverter circuit. For input logic at high, it gives output low and for input logic at low, it passes the clock signal. The proposed structure tries to keep the output logic at high when input is low instead of passing the clock signal as in case of reported 2PASCL.

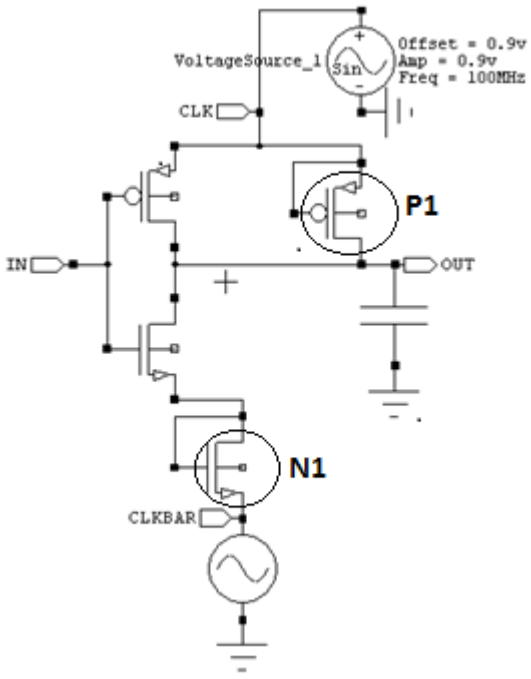

Fig. 1 Structure of 2PASCL

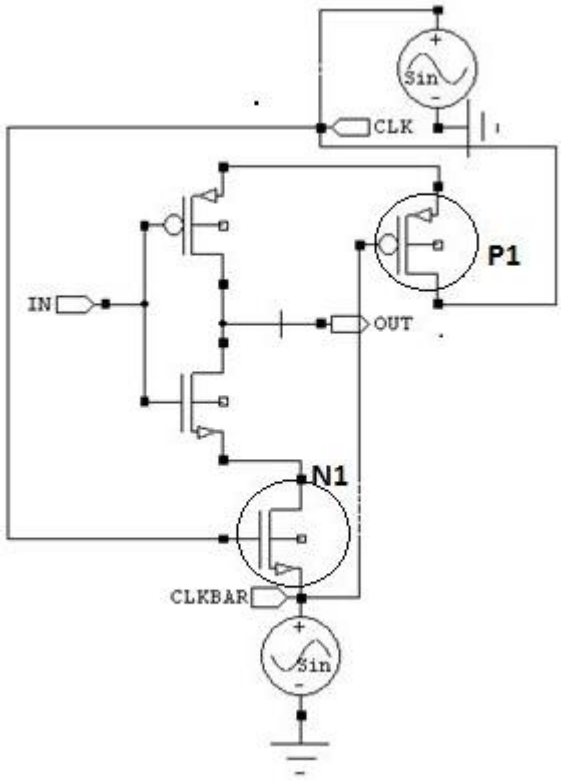

Fig. 3 Structure of proposed 2PASCL

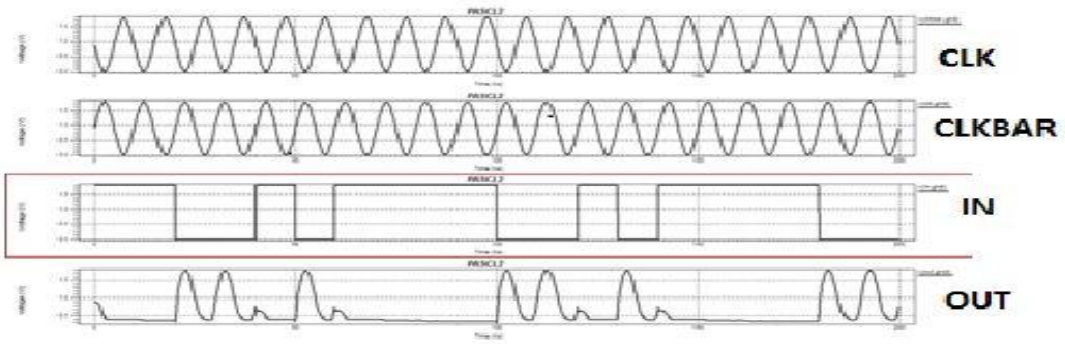

Fig.2 Simulation Waveform for 2PASCL Inverter

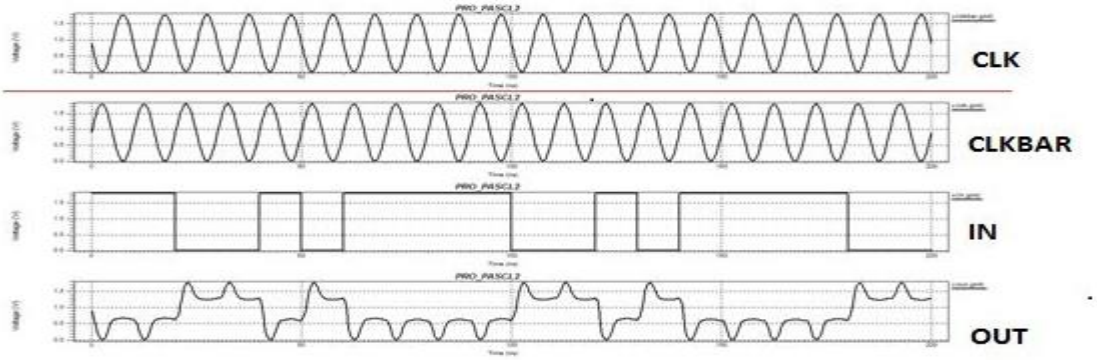

Fig. 4 Simulation Waveform for proposed 2PASCL Inverter

Proposed Two Phase Clocked Adiabatic Static CMOS Logic

The Proposed 2PASCL structure is shown in fig 3. Which consist of same number of transistor as that of reported one. The expression for adiabatic energy dissipation given as

$$E_{diss} = \frac{R}{T} C_L{}^2 V_{dd}{}^2 \quad (1)$$

Where R is resistor in charging and discharging path, C_L is the load capacitance, V_{dd} is the supply voltage, and T is charging time. From eq1 it is obvious that if we increase T, then energy dissipation can be reduced. Using this concept, the proposed circuit is modified in such a way that charging time is increased which results in less energy dissipation. The operation of the circuit is performed in two phases i.e. Evaluation phase and Hold phase.

Circuit Operation

Evaluation phase: In Evaluation phase CLK goes high and CLKBAR goes low, when output is at logic low and P1 transistor is on, output load capacitor is charged through P1 transistor and output reaches at logic high. Output load capacitor discharges through transistor N1 when output is high and causes the output state at low.

Hold Phase: In hold phase CLK goes low and CLKBAR goes high no transitions occur at the output if the transistor P1and N1 voltage reaches below the threshold voltage, both theP1 and N1 turn off. Due to the hold phase, dynamic switching is reduced and hence energy dissipation is reduced. The clock signal is sinusoidal and 180^0 phase shifted with each other. Each clock signal height is maintained at 1.8v. The substrate of PMOS and NMOS are connected to V_{dd} and ground. Fig 4 shows simulation waveform for proposed 2PASCL inverter at clock frequency of 100 MHz and input signal frequency at 50 Mhz. the details analysis of power dissipation, delay and power delay product shows that the proposed circuit perform best if the input signal frequency is half or doubled the clock signal frequency. The Proposed Inverter circuit saves 6.87% power over reported 2PASCL and 7.85% power over conventional CMOS logic at clock frequency of 100 MHz and input signal frequency of 50 MHz.

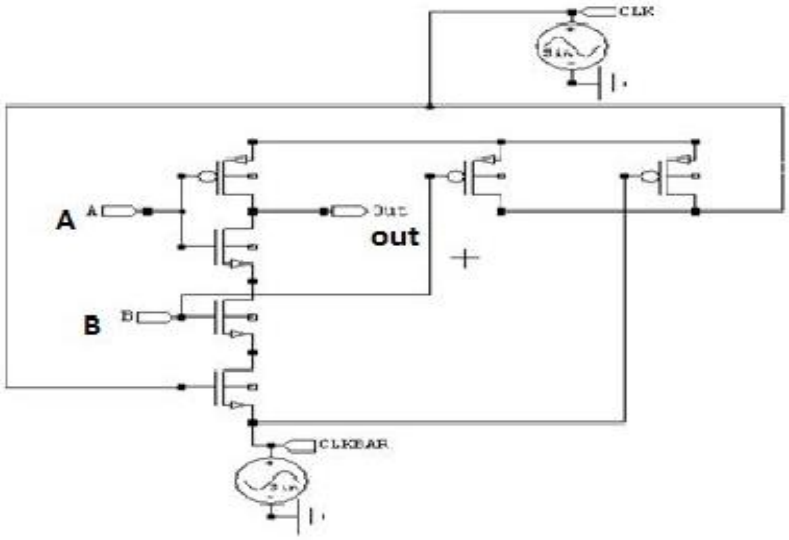

Fig.5 Design of NAND gate using proposed 2PASCL

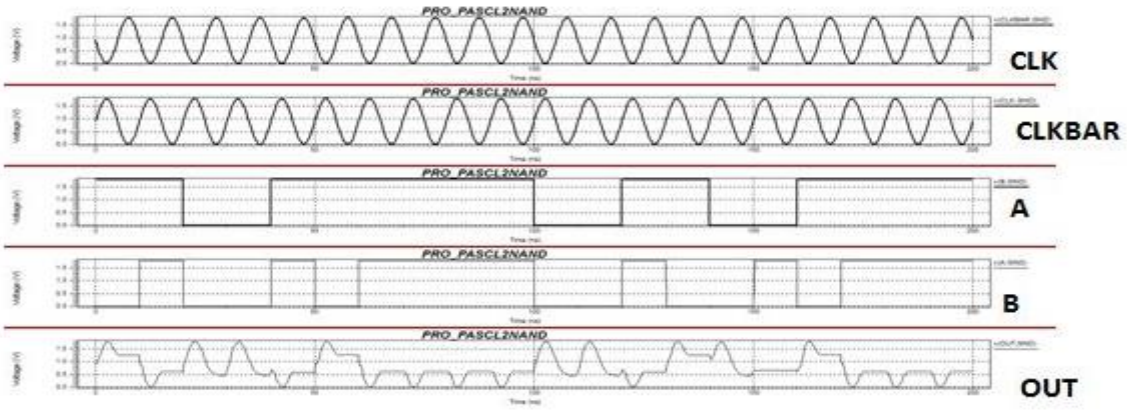

Fig. 6 Simulation Waveform for proposed 2PASCL NAND

COMBINATION CIRCUITS

We designed the basic circuits such as NAND, NOR and XOR which are required for design of any combinational circuits using both the logic style.

NAND Gate

NAND gate is the universal gate which is implemented using the basic equation $Y = \overline{AB}$, where Y is the output and A and B are its two input. The proper working of the circuit is examined by simulation waveform shown in fig 6. For input A and B, voltage level for logic high is 1.8v and 0v for logic low. The proposed NAND gate circuit saves 34.19% power over reported 2PASCL and 38.76 % power over conventional CMOS logic at clock frequency of 100 MHz and input signal frequency of 50 Mhz. simulation is carried out over the time period of 1ns to 100ns all the parameters and environment is maintained constant for comparison purpose.

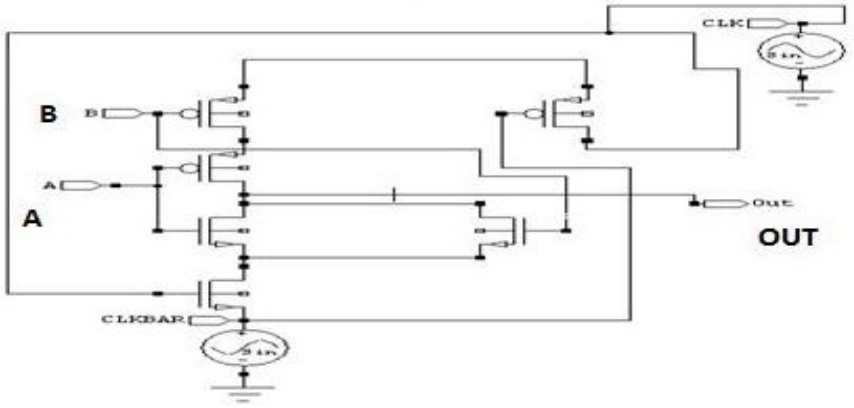

Fig.7 Design of NOR gate using Proposed 2PASCL

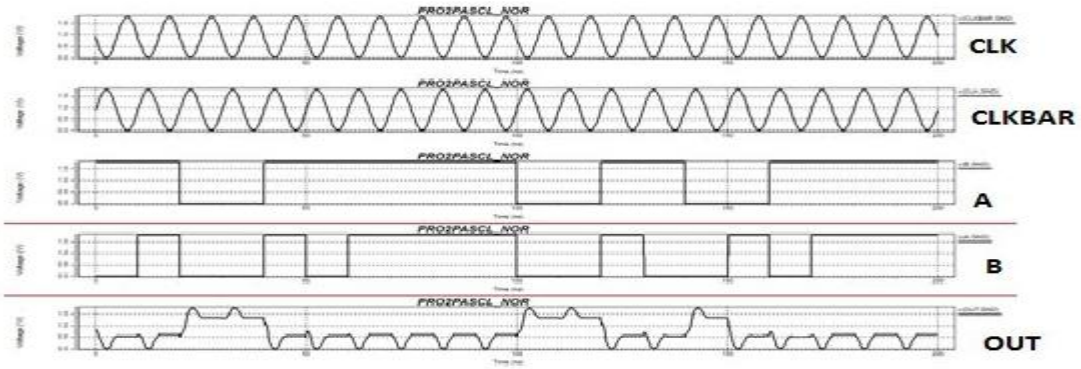

Fig 8. Simulation Waveform for proposed 2PASCL NOR

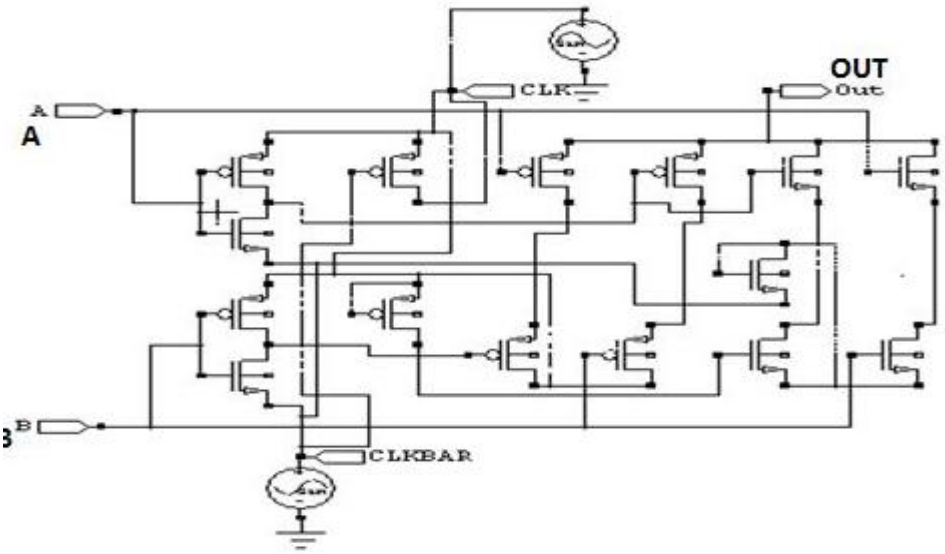

Fig 9 Design of XOR gate using proposed 2PASCL

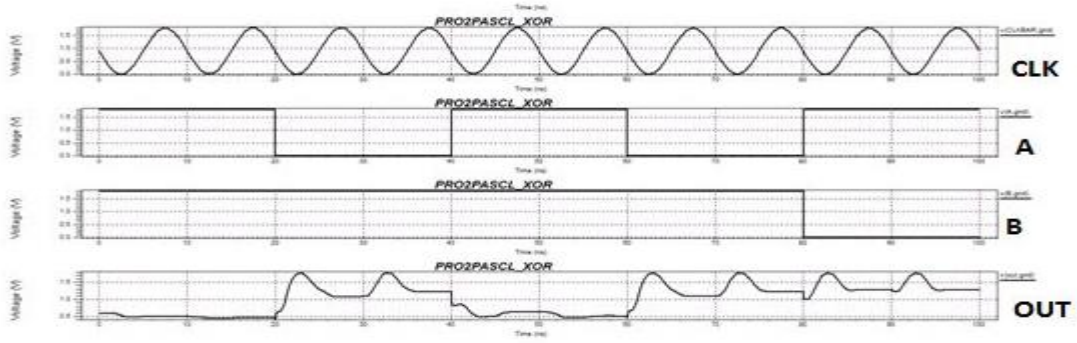

Fig 10. Simulation Waveform for proposed 2PASCL XOR

NOR gate

NOR gate is implemented using the basic equation $Y = \overline{A+B}$, where Y is the output and A and B are its two input. The simulation waveform is shown in fig 8. The proposed NOR gate circuit is saves 10.62% power over reported 2PASCL and 44.45% power over conventional CMOS logic at clock frequency of 100Mhz and input signal frequency of 50 Mhz.

XOR Gate

XOR gate is implemented using the basic logic equation. Simulations waveform for the circuit is shown in Fig. 10. The proposed XOR gate circuit saves 38.45% power over reported 2PASCL and 99% power over conventional CMOS logic at clock frequency of 100Mhz and input signal frequency of 50 Mhz.

RESULTS AND DISCUSSION

Comparative power, delay and Power Delay Product analysis has been done over a frequency range varying from 20MHz to 100MHz are summarized in the table below. The power delay product which is one of the figure of merit to measure the performance of digital circuits is also obtained in the analysis. The PDP for the proposed circuit such as NAND, NOR and XOR gives best results.

Table -1 Comparative Analysis for Inverter at Clock Frequency 100MHz

Frequency	Clock frequency 100MHz inverter								
	Power dissipation (uW)			*Delay (ns)*			*Power Delay Product (fJ)*		
	CMOS	*Reported[10]*	*Proposed*	*CMOS*	*Reported*	*Proposed*	*CMOS*	*Reported*	*Proposed*
20MHz	0.162	0.052	0.083	24.92	19.42	18.42	4.03	1.00	1.52
40MHz	0.433	0.093	0.101	12.42	19.72	19.88	5.37	1.83	2.00
50MHz	0.567	0.108	0.064	9.92	19.42	19.62	5.62	2.09	1.25
60MHz	0.694	0.179	0.203	7.92	11.66	11.77	5.49	2.08	2.38
80MHz	0.897	0.113	0.267	6.17	12.39	12.42	5.53	1.40	3.31
100MHz	1.035	0.134	0.109	4.92	9.42	9.65	5.09	1.26	1.05

Table-2 Comparative Analysis for Inverter at Clock Frequency 50MHz

Frequency	Clock frequency 50MHz inverter								
	Power dissipation (uW)			*Delay (ns)*			*Power Delay Product (fJ)*		
	CMOS	*Reported[10]*	*Proposed*	*CMOS*	*Reported*	*Proposed*	*CMOS*	*Reported*	*Proposed*
20MHz	0.162	0.042	0.034	24.92	39.12	39.42	4.03	1.64	1.34
40MHz	0.433	0.103	0.188	12.42	24.92	24.89	5.37	2.56	4.67
50MHz	0.567	0.154	0.061	9.92	19.55	19	5.62	3.01	1.15
60MHz	0.694	0.117	0.157	7.92	11.80	11.48	5.49	1.38	1.80
80MHz	0.897	0.297	0.212	6.17	4.80	4.64	5.53	1.42	0.98
100MHz	1.035	0.257	0.350	4.92	5.06	5.10	5.09	1.30	1.78

Table -3 Comparative Analysis for NAND Circuit

Frequency	Clock frequency 100MHz NAND								
	Power dissipation (uW)			*Delay (ns)*			*Power Delay Product (fJ)*		
	CMOS	*Reported[10]*	*Proposed*	*CMOS*	*Reported*	*Proposed*	*CMOS*	*Reported*	*Proposed*
20MHz	0.564	1.70	0.103	108.49	49.74	49.65	61.18	84.40	5.11
40MHz	1.67	1.75	0.0252	88.29	24.79	24.65	147.44	43.38	0.621
50MHz	2.64	2.33	0.0662	70.79	19.74	19.65	186.88	45.99	1.30
60MHz	3.62	1.67	0.059	56.79	15.74	15.65	205.57	26.33	0.923
80MHz	4.24	1.508	0.134	45.59	12.24	12.15	193.30	18.45	1.628
100MHz	5.69	1.79	0.012	35.79	9.74	6.65	203.64	17.43	0.0798

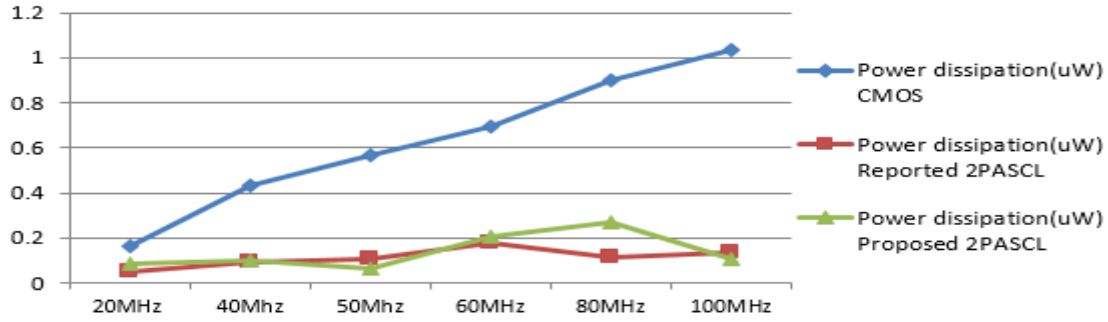

Fig. 11 Comparative power analysis for inverter at 100mhz clock frequency

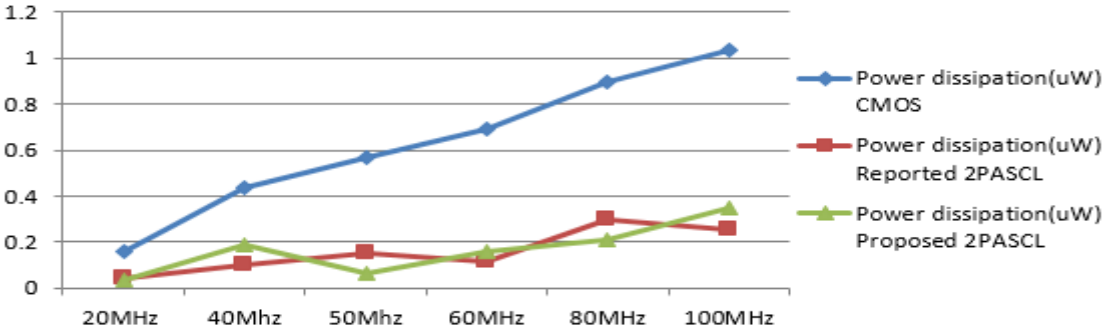

Fig. 12 Comparative Power Analysis for inverter at 50MHz clock frequency

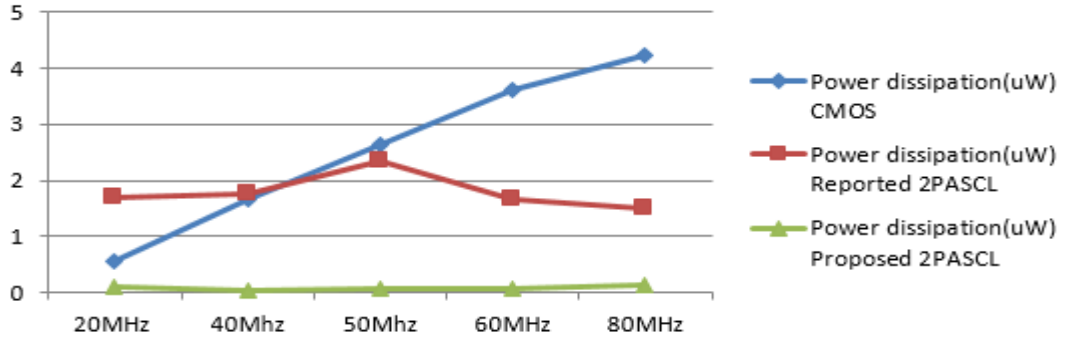

Fig. 13 Comparative Power Analysis for NAND circuit

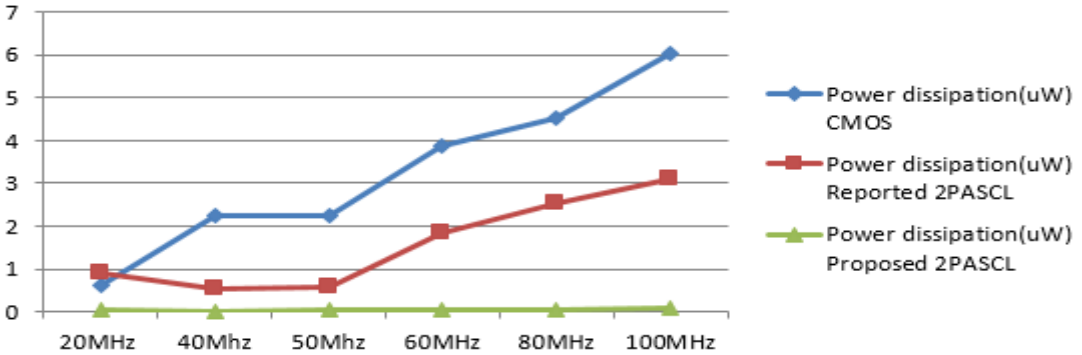

Fig. 14 Comparative Power Analysis for NOR circuit

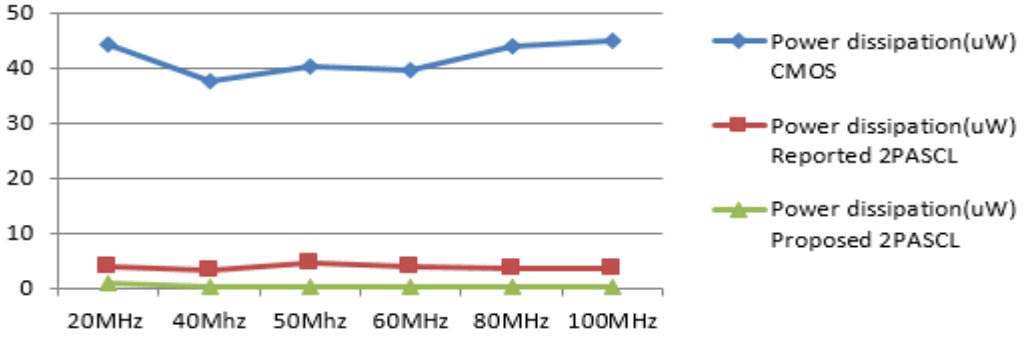

Fig.15 Comparative Power Analysis for XOR circuit

Table -4 Comparative Analysis for NOR Circuit

Frequency	Clock frequency 100MHz NOR								
	Power dissipation (uW)			*Delay (ns)*			*Power Delay Product (fJ)*		
	CMOS	*Reported[10]*	*Proposed*	*CMOS*	*Reported*	*Proposed*	*CMOS*	*Reported*	*Proposed*
20MHz	0.603	0.92	0.034	50.40	19.3	60.42	30.39	17.75	2.02
40MHz	2.23	0.54	0.0164	25.40	12.22	50.42	56.64	6.59	0.826
50MHz	2.25	0.57	0.0495	20.40	9.21	41.17	45.9	5.24	2.03
60MHz	3.87	1.82	0.0375	16.40	5.70	33.28	63.46	10.37	1.24
80MHz	4.53	2.51	0.0449	12.92	3.48	25.47	58.52	8.73	1.14
100MHz	6.05	3.10	0.0765	10.40	3.07	21.89	62.92	9.51	1.67

Table -5 Comparative Analysis for XOR circuit

Frequency	Clock frequency 100MHz XOR								
	Power dissipation (uW)			*Delay (ns)*			*Power Delay Product (fJ)*		
	CMOS	*Reported[10]*	*Proposed*	*CMOS*	*Reported*	*Proposed*	*CMOS*	*Reported*	*Proposed*
20MHz	44.07	3.77	0.801	24.74	54.65	53.89	1090.29	206.03	43.16
40Mhz	37.62	3.14	0.140	14.24	43.94	43.94	535.70	137.97	6.15
50Mhz	40.04	4.656	0.118	11.74	38.96	37.56	470.06	181.39	4.43
60MHz	39.47	3.928	0.246	9.74	26.97	26.12	384.43	105.93	6.42
80MHz	43.79	3.49	0.283	7.99	24.89	23.81	349.88	86.86	6.73
100MHz	44.85	3.61	0.308	6.79	19.10	18.23	304.53	68.95	5.61

CONCLUSION

This paper has proposed the Improved Two Phase Clocked Adiabatic Static CMOS logic (2PASCL) circuit and various combination logic circuits such as NAND, NOR and XOR. The comparative analysis over a frequency range from 20MHz to 100MHz for power, delay and Power Delay Product proves that the proposed logic gives less power dissipation compared to conventional CMOS and Reported 2PASCL. For inverter design it saves 7.85% of power over CMOS and 6.87% of power for 2PASCL. Paper also presents detailed delay analysis over a wide frequency range. The two complementary sinusoidal power clock is used whose peak to peak voltage is 1.8V. For the future work the proposed circuit can be analysed for sinusoidal power clock with peak to peak voltage of 0.9V.

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