Design of a Power Efficient D-Flip Flop using AVL Technique

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ABSTRACT

Power optimization is a very crucial issue in low voltage applications. This paper presents a design of D-Flip flop circuit using AVL techniques for low power operation. It reduces the value of total power dissipation of applying the adaptive voltage level at ground (AVLG) technology in which the ground potential is raised and adaptive voltage level of supply (AVLS) in which supply potential is increased. The main aim of the design is to investigate the power dissipation for D-Flip flop for the proposed design style. The simulation results show the there is a significant reduction in power consumption of this proposed cell with the AVL technique. The AVLS technique has less power dissipation 1.13 nwatts compared to AVLG technique 2.25 nwatts. The circuit is designed using H-Spice 130nm technology.

Key words: DFF, AVL, AVLS, AVLG, H-Spice, TSPC, VLSI

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INTRODUCTION

Sequential circuits are the logic circuits whose outputs at any instance of time depend not only on the present inputs but also on the past outputs. Sequential circuits are of two types (i) synchronous or clocked and (ii) synchronized or un-clocked. The simplest kind of sequential circuit is a memory cell that has two states. It can be either 1 or 0. Such two state sequential circuits are called flip-flops because they flip-from one state to another and then flop back [1].

Flip-flops are used as the memory elements which are the basic building blocks of an IC. They are used in many applications like parallel data storage, shift registers, frequency division and counters, etc. As synchronous flip-flops uses a master-clock generator, which generates a periodic train of clock pulses. This leads to huge power consumption of power in synchronous circuits [10]. So, by eliminating the unnecessary switching of the transistors with respect to the clock signal in memory elements we can reduce the power dissipation to a large amount. And also by avoiding un-wanted switching of internal transistors the power can be reduced. The adaptive voltage level Logic is a better way to implement circuits designed for low power applications [19].

Paired rationale has been generally utilized as a part of the electronic field [3]. It is customary and subsequently, more develop than various esteemed rationales. In any case, close by the blasting of the data and electronically industry, the lack of two fold circuits started to develop. It has been somewhat troublesome for a twofold rationale to fulfill requests from chip region, exchanging rate, power dispersal, and different angles all in the meantime [11]. Along these lines, numerous esteemed circuits are turning out to be progressively critical. Advanced circuits in each fast innovation are commonly benchmarked by the execution of static recurrence dividers which is perceived as at figure of merit for an advanced coordinated circuit process, on the grounds that a static recurrence divider uses the same essential flip-flop components found in more mind boggling consecutive circuits. Fast recurrence dividers are one of the key gadgets in estimation types of gear, microwave and satellite correspondence frameworks [12]. Along these lines, numerous diverse rapid static and element recurrence dividers taking into account different sorts of gadget innovation have been produced. Building a low power VLSI frameworks have developed as profoundly popular due to the quickly developing innovations in portable correspondence and calculation. The battery innovation does not propel at the same rate as the microelectronics innovation [18].

There is a restricted measure of force accessible for the portable frameworks. So architects are confronted with more requirements: fast, high throughput, little silicon region, and in the meantime, low power utilization. In this way building low power, superior circuits is of extraordinary hobby [9].
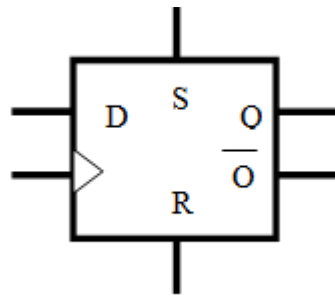
Fig 1D Flip-Flop Symbol

Wide usage of memory stockpiling frameworks and successive rationale in cutting edge hardware triggers an interest for superior and low-zone executions of fundamental memory parts. A standout amongst the most essential state-holding components is the D-Flip-Flop (DFF) [2]. Different DFF circuits were looked into and exhibited in the writing, expecting to accomplish an ideal configuration in terms of deferral, force and zone. Some effective strategies were created and embraced by creators for a mixed bag of innovations [17].

The D flip-failure catches the D's estimation information at an unmistakable bit of the clock cycle, (for example, the rising edge of the clock) [6]. That caught worth turns into the Q yield. At different times, the yield Q does not change. The D flip-failure can be seen as a memory cell, a zero-request hold, or a postponement line [20].

Clock	D	Q_{next}
Rising Edge	0	1
Non-Rising	X	Q

'X' denotes a *Don't care* condition, meaning the signal is irrelevant

Reenactment of the locks and flip-failures got by utilizing diverse outline styles makes this investigation more troublesome in attempting to accomplish predictable and equivalent results. There are two noteworthy results created [13]:

1) The meaning of the significant arrangement of parameters to be measured furthermore, manages for weighting their significance;

2) An arrangement of pertinent re-enactment conditions, which underscore the parameters of the hobby.
The re-enactment and enhancement methodology have elite as the essential objective, however, we have likewise paid consideration on the conceivable diminishes in force utilization, given that the impediment in execution is generally forced by the accessible force spending plan [4].

D- FLIP FLOP USING AVLG TECHNIQUE

The Fig. 2 shows the basic block diagram of TSPC based D Flip-flop. In AVLG technique, combinations of 1-N-MOS & 2-P-MOS transistors are connected in parallel. So that an input clock pulse is applied at the NMOS of circuit of AVLG and rest of all P-MOS are connected to ground [5].
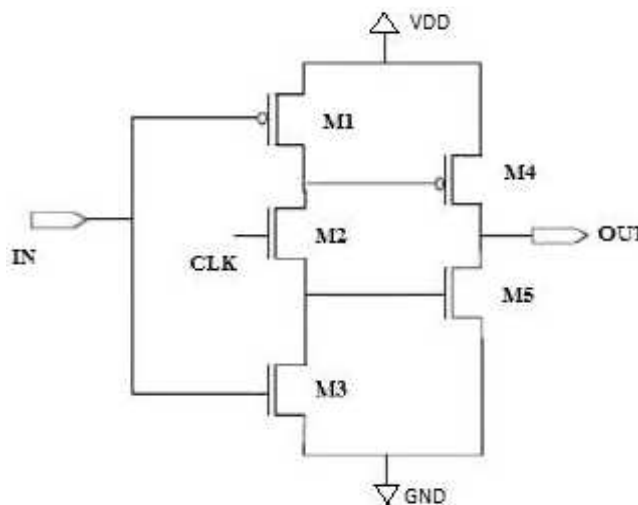

Fig. 2 Basic TSPC based D Flip-Flop [16]

This AVLG circuit is connected at the ground terminal of conventional one by removing ground. This ground terminal is connected to the AVLG circuit. Fig. 3 shows the circuit diagram of D Flip Flip-flop designed using AVLG technique [7].
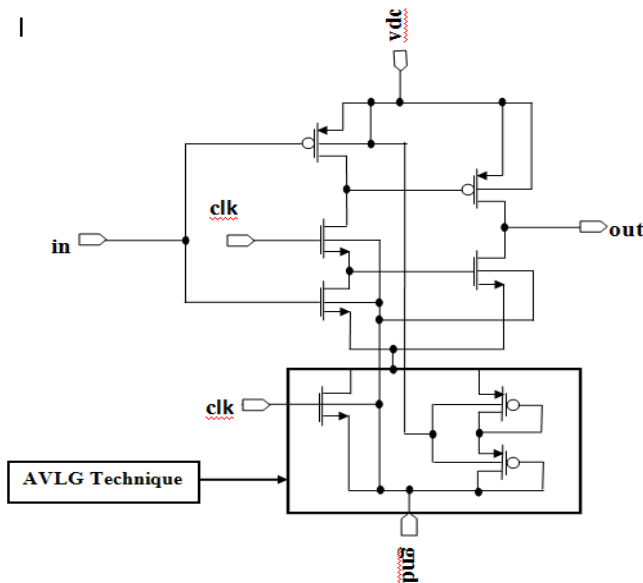
D- FLIP FLOP USING AVLS TECHNIQUE

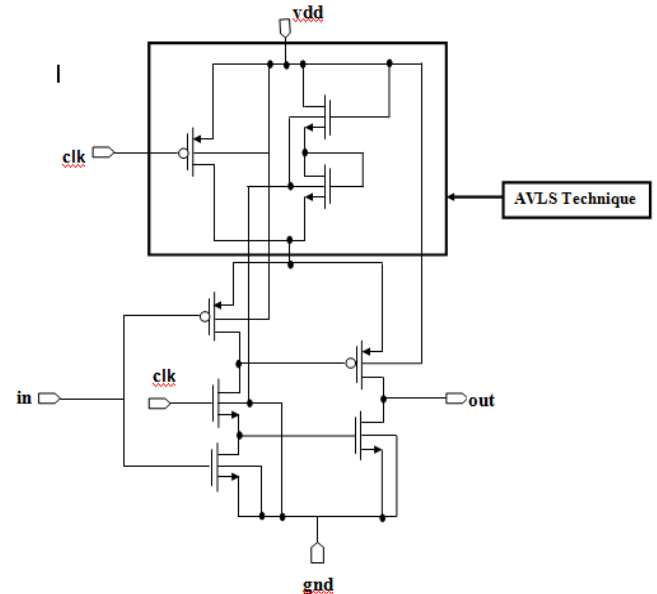**Fig. 3 D Flip-flop designed using an AVLG technique [14]**

Fig. 4 D Flip-flop designed using AVLS technique [15]

SIMULATION RESULTS

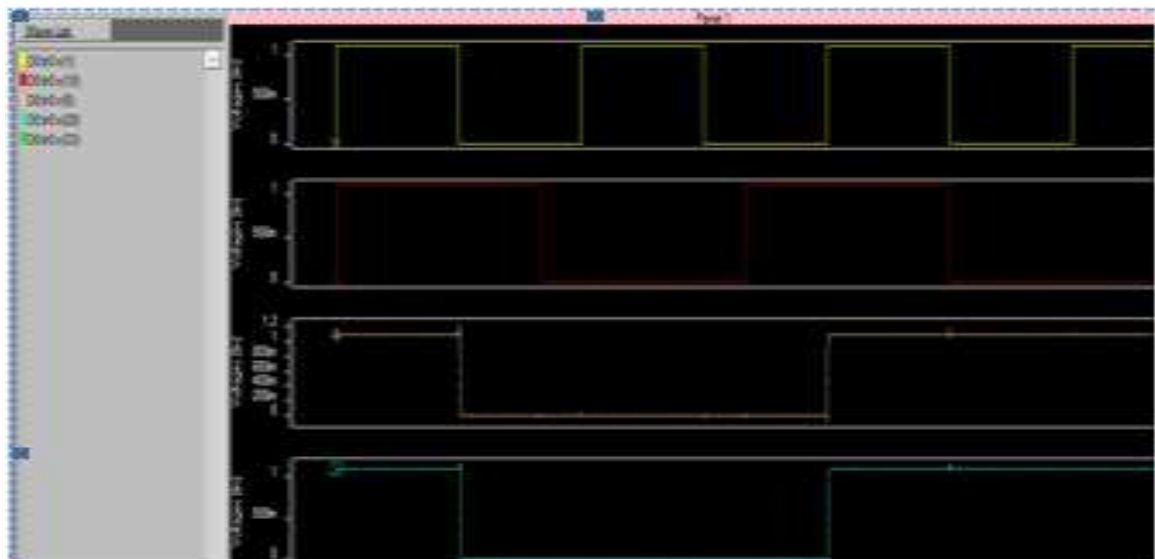| Power Dissipation	AVLG Technique	AVLS Technique
	2.25 nwatts	1.13 nwatts

Fig.5

CONCLUSION

The D Flip-flop is designed with H-Spice 130nm technology. For low power applications the power reduction technique is done to obtain optimum results. Minimization of power consumption is essential for high performance VLSI systems. The simulation results clearly explain the reduction in the power consumption by incorporating by AVL techniques that is AVLG and AVLS technique. The AVLS technique has less power dissipation 1.13 nwatts compared to AVLG technique 2.25nwatss.

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