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Design of Low-Power and High-Speed Opamp Integrated Circuits Using Silicon Nanowire Transistors

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ABSTRACT

SNTs (surrounding-gate nanowire transistors) are good candidates to implement low power electronic devices. They provide full gate control over the channel and minimize short channel effects. Design of a high-speed opamp is presented in this paper. It consists of two amplifying stages and an output buffer and is frequency compensated for stable operation. Transistors used have 10nm channel length and 2nm channel radius. The amplifier operates from 1.8V supply and has a voltage gain of 40dB and a phase margin of 42°. The current gain cutoff frequency of the amplifier is 5.1THz and it provides 40dB common mode rejection ratio and 54dB power supply rejection ratio with a slew-rate of 2V/ns. The amplifier area is 320nm by 250nm.

Key words: Nanowire, field effect transistors, amplifiers, gain, bandwidth, small-signal, opamps

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INTRODUCTION

Semiconductor technologies and integrated circuits have enormously contributed to the progress of communications, electronics and computer industries. Since 1960's, the number of transistors have doubled in systems realized by every new generation of the VLSI technologies while the feature size of the transistors has reduced as described by Moore's law [1]. The small feature size of the transistors used to realize complex integrated circuits help to in-crease the functionality of these systems while reducing their cost. The increased functionality is achieved by integrating the digital back-end circuits of a communication system with Analog and RF (radio frequency) circuits on the same silicon substrate. The small feature size also enables the various circuits to operate at higher speeds and transfer more information from a transmitter to a receiver [2-3].

Recently, the downscaling of the Bulk MOSFETs (metal oxide semiconductor field effect transistors) have reached the nanometer range, which is close to the physical limit predicted by the ITRS (industrial technology roadmap for semiconductors) [4]. After the Bulk MOSFETS reach a channel length of less than 45nm only a few atomic layers will exist among the transistor junctions, causing many undesired short channel and reliability effects. Therefore, other alternative silicon based transistor structures with high speed and low power characteristics are needed.

A variety of silicon compatible technologies such as SOI (silicon on insulator) MOSFETs, FinFETs and nanotube FETs are being designed and scaled down to nanometer dimensions [5-10]. Due to the quantum-level issues associated with these nanoscale devices, the main stream fabrication of these transistors has been hindered and the high frequency behaviour and accurate modelling of these transistors have not completely been investigated [11-14]. SNTs (surrounding gate nanowire transistors) are among the most promising nanoscale silicon compatible transistors which offer high performance and high level of integration while exhibiting better downscaling characteristics [15-18].

Increasing the performance, functionality and throughput of the wireless communication systems are the main reasons to increase the operating frequency and to reduce the feature size of the mainstream semiconductors. The continuous shrinking of the conventional Bulk MOSFETs (metal oxide semiconductor field effect transistors) has introduced many undesirable short channel effects and therefore, alternative silicon compatible transistor devices such as SOI (silicon on insulator) MOSFETs, FinFETs and nanotube FETs have been designed and downscaled to nanometer dimensions for improved performance. Soon after the mainstream MOSFETs reach their physical limits and exhibit undesired performance, the choice of an alternative technology will be invaluable for industries to find a suitable replacement for conventional Bulk MOSFETs.

Among these structures, SNTs seem to have the least short channel effects. Similar to the industrial trends of the semiconductor technologies, the prior work of the authors on SNTs concentrated on optimizing these transistors for digital applications and exploring their functionality using simple transistor models. The accurate modelling and the high speed properties of these devices for Analog applications are investigated by authors [19]. This paper presents an accurate modelling of these transistors using BSIM-SOI compatible modelling and the detailed design of a high speed and low power operational amplifier using SNTs.

DESIGN AND ANALYSIS

The three dimensional view and the corresponding parasitic components of SNT are shown in Fig.1. Only, the dominant parasitics are considered to simplify the circuit model. The intrinsic transistor is modelled using a BSIM-SOI compatible model to ensure all the input and output transfer characteristics of the circuit and device simulators match each other. The parasitic capacitance between the source contacts and the metal gate is denoted as C_{gs2} in the figure. The parasitic capacitance C_{gs1} between the metal gate and the concentric source contact and the junction well is the largest dominant capacitors of the SNT device. The gate and drain capacitors (C_{gd1} and C_{gd2}) and the drain and source capacitors (C_{ds1} and C_{ds2}) can be lumped into C_{gd} and C_{ds}, respectively. Compared to planar Bulk transistors, C_{gd} is very small and there is no junction to bulk capacitance, therefore, C_{ds} is quite linear. The well resistance R_s can be quite large and is the major drawback of the vertical SNTs compared with planar transistors. The magnitude of this resistance can be reduced drastically by placing a concentric (ring shape) source contact in parallel with the well, as shown in the figure. If the transistor is properly designed to ensure $G_s \gg g_m \gg g_{ds}$ (where g_m is the intrinsic transconductance and g_{ds} is the intrinsic output conductance of the transistor), the performance of the nanowire transistors in analog circuits exceeds those of planar transistors. This will be shown in the next sections.

The simplified parasitic components associated with NMOS and PMOS SNTs are shown in Fig.2 (a) and (b). For accurate circuit level simulations, the intrinsic SNTs (M_n and M_p) are modelled using BSIM-SOI. For simplified hand calculations and finding the AC parameters of the amplifiers designed using SNTs, the linearized small-signal model shown in Fig.3 can be used. Using this model at low frequencies, the DC voltage gain and output resistance of various amplifier stages can be calculated.

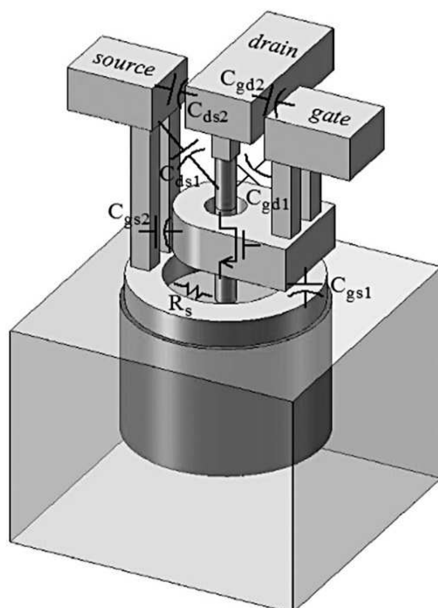

Fig. 1 SNT 3D View

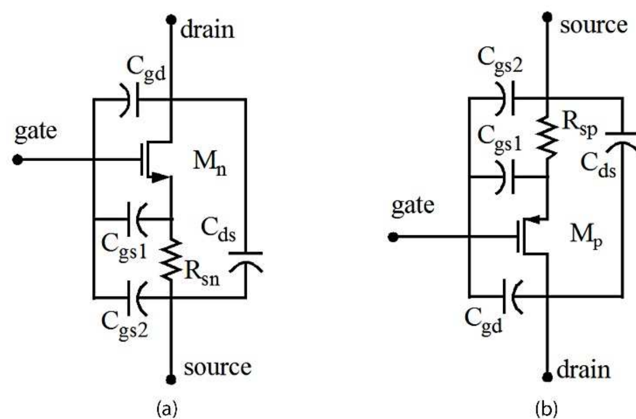

Fig.2 Simplified Parasitic Components Associated with (a) NMOS and (b) PMOS SNT

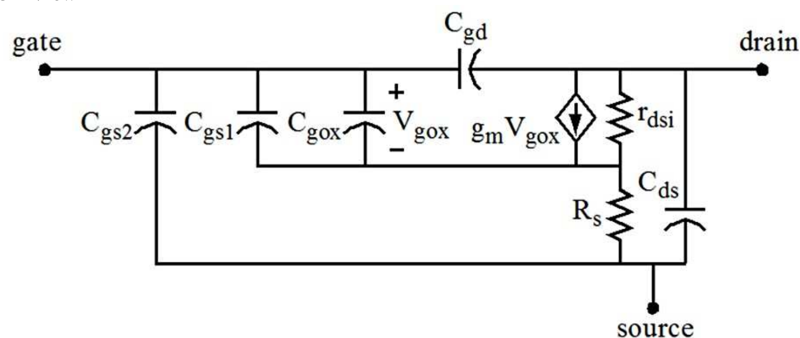

Fig.3 Linearized Small-Signal Model of SNT

Operational amplifiers are one of the most important building blocks of analog integrated circuits. Differential pair amplifiers, common source amplifiers, cascode amplifiers and common drain amplifiers are the basic building blocks of any opamp, as shown in Fig.4. Before designing an opamp and measuring its characteristics, the performance of each of these basic amplifiers will be investigated. The low frequency small signal model of the differential pair amplifier designed using SNTs is shown in Fig.5. The differential pair amplifier is usually used in the first stage of opamps.

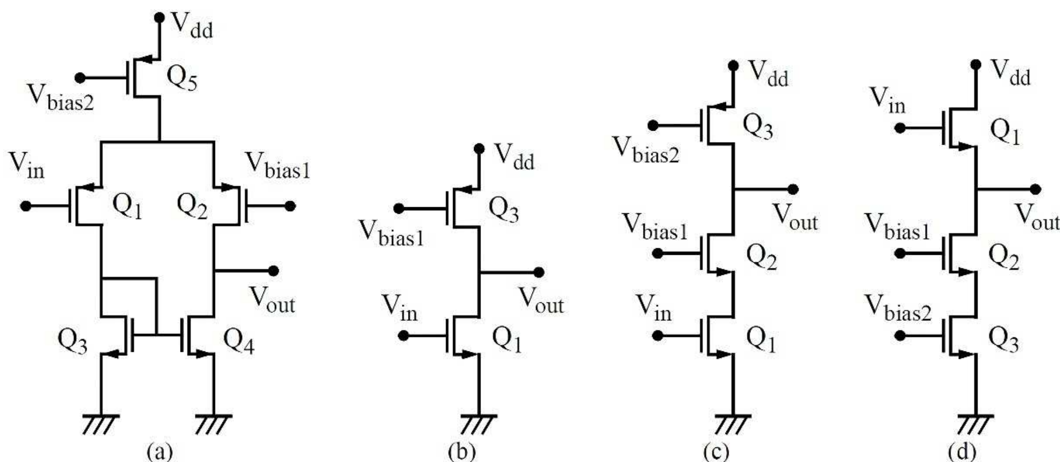

Fig.4 (a) Differential Pair, (b) Common Source, (c) Cascode and (d) Common Drain Amplifiers

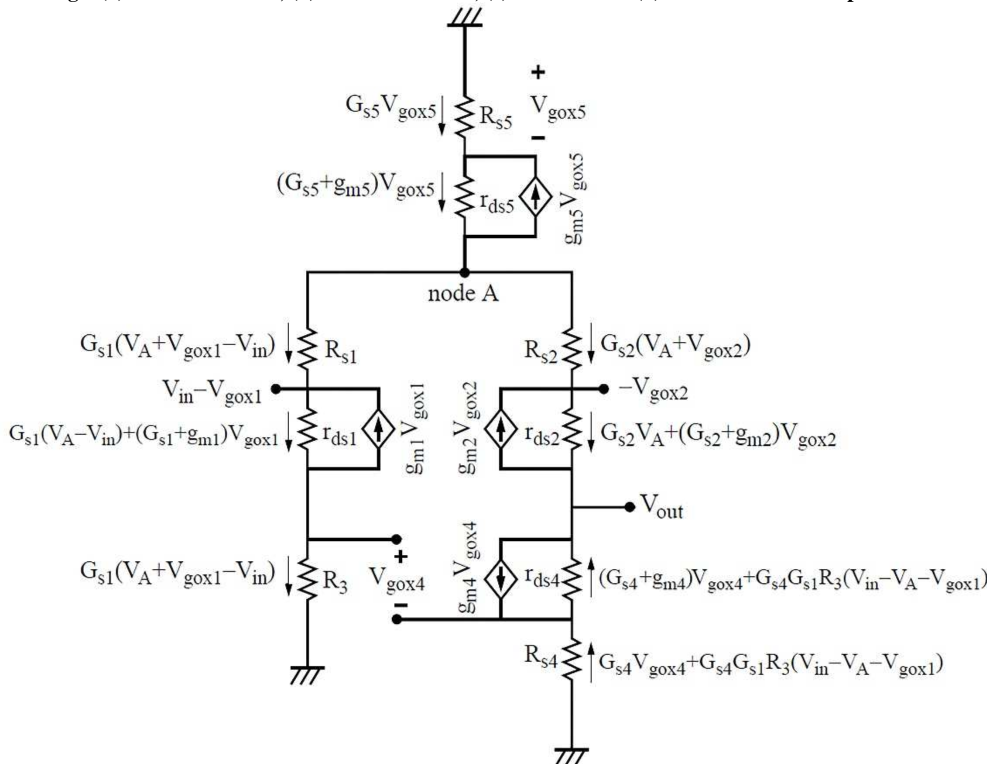

Fig. 5 The Low Frequency Small Signal Model of the Differential Pair Amplifier

The resistor R_3 is given by

$$R_3 = R_{s3} + \left(r_{ds3} \,||\, \frac{1}{g_{m3}}\right) \tag{1}$$

The voltage at node A, V_A, is given by

$$V_A = -[1 + r_{ds5}(G_{s5}+g_{m5})]V_{gox5} \tag{2}$$

The output voltage V_{out} can be expressed by

$$V_{out} = -[\,1 + r_{ds4}(G_{s4} + g_{m4})]V_{gox4} - G_{s1}R_3[1 + r_{ds4}G_{s4}](V_{in} - V_A - V_{gox1}) \tag{3}$$

And

$$V_{out} = -r_{ds2}G_{s2}V_A - [1 + r_{ds2}(G_{s2} + g_{m2})]V_{gox2} \tag{4}$$

The KCL at output branch results in

$$G_{s2}\left(V_A + V_{gox2}\right) = G_{s4}V_{gox4} + G_{s4}G_{s1}R_3\left(V_{in} - V_A - V_{gox1}\right) \tag{5}$$

The KVL at input branch results in

$$V_{in} - V_{gox1} = r_{ds1}G_{s1}(V_A - V_{in}) + r_{ds1}(G_{S1} + g_{m1})V_{gox1} + R_3G_{S1}(V_A + V_{gox1} - V_{in}) \tag{6}$$

The KCL at node A results in

$$G_{s5}V_{gox5} = G_{s2}\left(V_A + V_{gox2}\right) + G_{s1}\left(V_A + V_{gox1} - V_{in}\right) \tag{7}$$

The voltage gain of the differential pair amplifier is given by

$$\frac{V_{out}}{V_{in}} = \frac{gm2\, rds2 + \frac{r_{ds2}(g_{m2}+G_{s2})}{r_{ds5}\, G_{s2}}}{1 - \frac{g_{m2}\, r_{ds2}\left[r_{ds1}(g_{m1}+G_{s1}) + G_{s1}\left(R_{s3}+\frac{r_{ds3}}{1+g_{m3}\, r_{ds3}}\right)\right]}{g_{m1}\, r_{ds1}\, G_{s1}\, G_{s4}\, r_{ds4}\left(R_{s3}+\frac{r_{ds3}}{1+g_{m3}\, r_{ds3}}\right)}} \tag{8}$$

For $G_s \gg g_m \gg g_{ds}$, the voltage gain is approximately given by

$$\frac{V_{out}}{V_{in}} \approx gm2\, rds2 \tag{9}$$

The resistance seen from drain of Q_4 transistor of the differential pair amplifier is given by

$$R_{04} = \frac{g_{m2}r_{ds2} + \frac{g_{m1}G_{s1}r_{ds1}r_{ds2}(G_{s2}+g_{m2})}{G_{s2}\left(r_{ds1}(G_{s1}+g_{m1}) + G_{s1}\left(R_{s3} + \frac{r_{ds3}}{1+g_{m3}r_{ds3}}\right)\right)}}{\frac{g_{m1}r_{ds1}G_{s1}}{r_{ds1}(G_{s1}+g_{m1}) + G_{s1}\left(R_{s3} + \frac{r_{ds3}}{1+g_{m3}r_{ds3}}\right)}} \tag{10}$$

and the resistance seen from drain of Q_2 transistor of the differential pair amplifier is given by

$$R_{02} = \frac{\frac{r_{ds}(G_{s4}+g_{m4})}{G_{s4}}\left[g_{m2}r_{ds2} + \frac{g_{m1}G_{s1}r_{ds1}r_{ds2}(G_{s2}+g_{m2})}{G_{s2}\left(r_{ds1}(G_{s1}+g_{m1})+G_{s1}\left(R_{s3}+\frac{r_{ds3}}{1+g_{m3}r_{ds3}}\right)\right)}\right]}{\frac{g_{m1}r_{ds1}G_{s1}\left(g_{m4}r_{ds4}\left(R_{s3}+\frac{r_{ds3}}{1+g_{m3}r_{ds3}}\right)+\frac{r_{ds2}(G_{s2}+g_{m2})}{G_{s2}}\right)}{r_{ds1}(G_{s1}+g_{m1})+G_{s1}\left(R_{s3}+\frac{r_{ds3}}{1+g_{m3}r_{ds3}}\right)} + g_{m2}r_{ds2}} \tag{11}$$

For $G_s \gg g_m \gg g_{ds}$, the output resistance is approximately given by

$$R_{out} = R_{o4} \,||\, R_{o2} \approx \left[r_{ds}\left(1 + \frac{g_{m2}}{g_{m1}}\right)\right] || \, r_{ds4} \tag{12}$$

To achieve high accuracy in the transfer functions of various analog circuits such as switch capacitor filters and amplifiers, it is important that opamps provide a voltage gain higher than 1000. Due to limited voltage gain of the differential pairs, another amplifying stage must be added to satisfy the high gain requirement of the opamp. This second stage can also be used to improve the phase margin of the opamp and to ensure a stable operation while using the opamp in the closed loop.

The common source amplifiers are usually used in the second stage of an opamp and function as the Miller compensating stage. The low frequency small signal model of the common source amplifier realized using SNTs is shown in Fig.6.

The KCL at output branch results in

$$G_{s2}V_{gox2} = G_{s1}\left(V_{\text{in}} - V_{gox1}\right) \tag{13}$$

The output voltage V_{out} can be expressed by

$$V_{out} = (1 + r_{ds1}G_{s1})V_{in} - [1 + r_{ds1}(G_{s1} + g_{m1})]V_{gox1} \tag{14}$$

And

$$V_{out} = -[1 + r_{ds2}(G_{s2} + g_{m2})]V_{gox2} \tag{15}$$

The voltage gain of the common source amplifier is given by

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}\, r_{ds1}[1 + r_{ds2}(G_{s2} + g_{m2})]}{[1 + r_{ds2}(G_{s2} + g_{m2})] + \frac{G_{s2}}{G_{s1}}[1 + r_{ds1}(G_{s1} + g_{m1})]} \tag{16}$$

For $G_s \gg g_m \gg g_{ds}$, the voltage gain is approximately given by

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = -\mathrm{g_{m1}}(\mathrm{r_{ds1}} \,||\, \mathrm{r_{ds2}}) \tag{17}$$

The intrinsic gain $g_m.r_{ds}$ of the SNTs can be as high as 15 for a common source amplifier which is not enough to be used in the Miller stage of the opamp. The SNTs have very high unity-gain cutoff frequency and very low current handling capability. Therefore, using a large Miller capacitance is not feasible to achieve frequency compensation and other amplifier structures which provide much larger gain need to be investigated for use in the Miller stage.

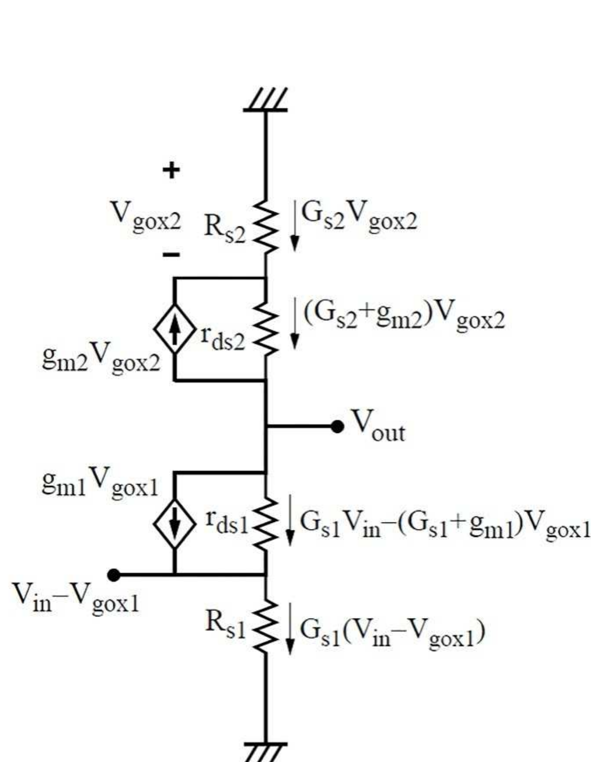

Fig.6 The Low Frequency Small Signal Model of the Common Source Amplifier

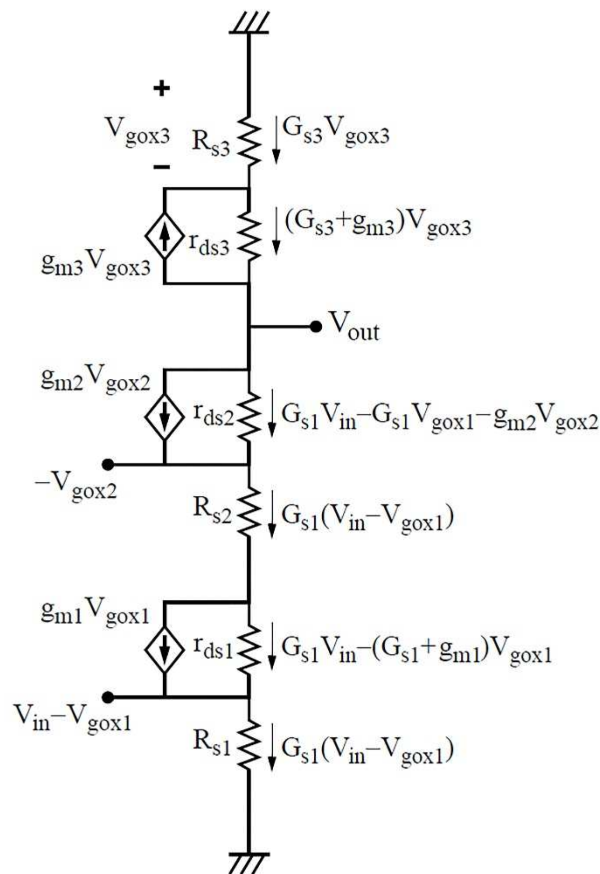

Fig.7 The Low Frequency Small Signal Model of the Cascode Amplifier

A cascade amplifier provides inverting gain as a common source amplifier, but, with a much larger gain. The low frequency small signal model of the cascade amplifier is shown in Fig.7.

The KCL at output branch results in

$$G_{s3}\, V_{gox3} \;= G_{s1}(V_{in} - \; V_{gox1}) \tag{18}$$

The output voltage V_{out} can be expressed by

$$V_{out} \;= -[1 + r_{ds3}(G_{s3} + g_{m3})]\; V_{gox3} \tag{19}$$

And

$$V_{out} = r_{ds2}G_{s1}V_{in} - r_{ds2}G_{s1}V_{gox1} - [1 + r_{ds2}g_{m2}]V_{gox2} \tag{20}$$

Where

$$V_{gox2} = \; -\big(1 + G_{s1}(r_{ds1} + \; R_{s2})\big)V_{in} + (1 + G_{s1}(r_{ds1} + R_{s2}) + g_{m1}r_{ds1})V_{gox1} \tag{21}$$

The voltage gain of the cascode amplifier is given by

$$\frac{v_{out}}{v_{in}} = \frac{-G_{s1}[1 + r_{ds3}(G_{s3} + g_{m3})][(1 + g_{m2}r_{ds2})\big(2R_{s1} + 2R_{s2} + r_{ds1}(2 + g_{m1}R_{s1})\big)]}{G_{s3}\big[(1 + g_{m2}r_{ds2})\big(R_{s1} + R_{s2} + r_{ds1}(1 + g_{m1}R_{s1})\big) - r_{ds2}\big] - 1 - r_{ds3}(G_{s3} + g_{m3})} \tag{22}$$

For $G_s \gg g_m \gg g_{ds}$, the voltage gain is approximately given by

$$\frac{V_{out}}{V_{in}} = \frac{-2g_{m2}\, r_{ds1}r_{ds2}\, r_{ds3}\, G_{s1}}{g_{m1}g_{m2}r_{ds1}r_{ds2}\, R_{s1} - r_{ds3}} \tag{23}$$

Which can be very high due to the denominator. The output resistance of the cascode amplifier is given by

$$R_{out} = [R_{s2} + g_{m2}r_{ds1}r_{ds2}(1 + \; g_{m1}R_{s1})]||[r_{ds3}(1 + \; g_{m3}R_{s3})] \tag{24}$$

For $G_s \gg g_m \gg g_{ds}$, the output resistance is approximately given by

$$\mathrm{R_{out}} \approx \mathrm{r_{ds3}}(1 + \mathrm{g_{m3}}\; \mathrm{R_{s3}}) \tag{25}$$

The opamp needs to drive the capacitive loads. Therefore, it is very important to isolate the operation of the Miller stage and the load using a buffer stage designed using a common drain amplifier. The low frequency small signal model of the common drain buffer amplifier realized using SNTs is shown in Fig.8.

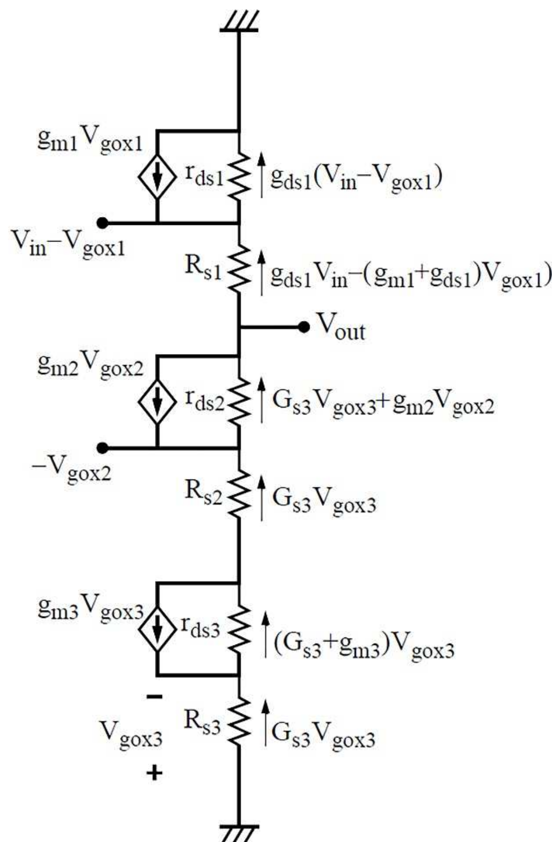

Fig.8 The Low Frequency Small Signal Model of the Common Drain Amplifier

The KCL at output branch results in

$$G_{s3}V_{gox3} = -g_{ds1}V_{in} + (g_{ds1} + g_{m1})V_{gox1} \quad (26)$$

The output voltage V_{out} can be expressed by

$$V_{out} = (1 + R_{s1}g_{ds1})V_{in} - (1 + R_{s1}(g_{m1} + g_{ds1}))V_{gox1} \quad (27)$$

And

$$V_{out} = -(1 + r_{ds2}\, g_{m2})V_{gox2} - G_{s3}\, r_{ds2}\, V_{gox3} \quad (28)$$

Where

$$V_{gox2} = -(1 + G_{s3}(r_{ds3} + R_{s2}) + g_{m3}r_{ds3})V_{gox3} \quad (29)$$

The voltage gain of the cascade amplifier is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}[-r_{ds2} + (1 + g_{m2}r_{ds2})(r_{ds3} + R_{s2} + R_{s3} + g_{m3}r_{ds3}R_{s3})]}{1 + (g_{m1} + g_{ds1})(R_{s1} - r_{ds2} + (1 + g_{m2}r_{ds2})(r_{ds3} + R_{s2} + R_{s3} + g_{m3}r_{ds3}R_{s3}))} \quad (30)$$

For $G_s \gg g_m \gg g_{ds}$, the voltage gain is approximately given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1}} \quad (31)$$

Which is very close to unity. The output resistance of the cascode amplifier is given by

$$R_{out} = \left[R_{s1} + \left(r_{ds1} \,||\, \frac{1}{g_{m1}}\right)\right] || \, [g_{m2}r_{ds2}r_{ds3}] \quad (32)$$

For $G_s \gg g_m \gg g_{ds}$, the output resistance is approximately given by

$$R_{out} \approx {}^{1}/_{g_{m1}} \quad (33)$$

And is very small. Using differential-pair, common-source and buffer amplifiers studied above, the overall low frequency voltage gain of the opamp is given by

$$\frac{V_{out}}{V_{in}} \approx g_{m34}r_{ds34} \times \frac{-2g_{m42}r_{ds41}r_{ds42}r_{ds43}G_{s41}}{g_{m41}g_{m42}r_{ds41}r_{ds42}R_{s41} - r_{ds43}} \times \frac{g_{m53}}{g_{m53} + g_{ds53}} \quad (34)$$

The location of the first pole of the opamp is given by

$$f_l \approx \frac{1}{2\pi[C_1 \times \frac{2g_{m42}\ r_{ds41}\ r_{ds42} r_{ds43}\ G_{s41}}{g_{m41}\ g_{m42}\ r_{ds41}\ r_{ds42} R_{s41} - r_{ds43}} \times (\ [r_{ds34}\left(1 + \frac{g_{m34}}{g_{m32}}\right)] \| \ r_{ds31})]} \tag{35}$$

and the location of the second pole of the opamp, determined by the load capacitor, is given by

$$f_H \approx \frac{g_{m53}}{2\pi C_1} \tag{36}$$

The opamp slew rate (SR) is given by

$$SR \approx \frac{I_{ds33}}{C_1} \tag{37}$$

MEASUREMENT

Using the analysis performed so far, a good choice of realizing a high performance SNT opamp involves using the first stage differential pair amplifier followed by the second stage cascode amplifier and finally using the buffer stage, as shown in Fig.9.

The transient and frequency response of the SNT differential pair amplifier is shown in Fig.10. The amplifier provides a gain of 16 with the first pole located at 100GHz and the second pole located at 100THz. The biasing control resistance R_0 is adjusted to create a reference current of 670μA in the current mirror circuit. Therefore, the drain-source currents of the biasing transistors I_{ds13}, I_{ds23}, I_{ds43} and I_{ds51} are 670μA and I_{ds33} is 1.4mA.

The impact of the Miller capacitance on the location of the poles and the comparison of the compensated and uncompensated opamps are shown in Fig.11. The lead compensation realized by using series combination of resistor R1 and capacitor C1 helps to improve the unity voltage gain cutoff frequency of the opamp without dissipating any power.

The layout of the opamp is shown in Fig.12. The main transistors of the input differential pair amplifier are realized by parallel combination of three p-type SNTs to ensure a large transconductance and the possibility to realize the second Miller stage by n-type SNTs. The resistor R_0 is used to control the biasing current of the opamp and is realized by using an n-well implantation with 8nm width and 320nm length dimensions. The opamp frequency compensation is achieved by using C_1 and R_1 components. The C_1 Capacitor is realized using metal-1 and metal-2 layers with 36nm spacing, 150nm width and 63nm length dimensions. The resistor R_1 is realized by using an n-well implantation with 8nm width and 48nm length dimensions. The width of the metal interconnects are selected to be 14nm to reduce their resistivity and four parallel vias are used to connect metal-1 and metal-2 layers to minimize the signal loss. Each via with 4nm by 4nm dimension and 36nm height has a resistance of 400Ω. Each overlap capacitance between metal-1 and metal-2 routing interconnects is 0.2aF for 14nm by 14nm dimension and 36nm height. The layout area of the opamp including the biasing circuit and all compensation components is x=330nm and y=250nm.

The frequency response of the two-stage opamp is shown in Fig.13. The designed opamp has a very high unity voltage gain cutoff frequency of 5.1THz and only dissipates 7.2μW. The opamp has a phase margin better than 90° for frequencies less than 1THz and achieves a very stable operation.

The open loop transient response of the opamp is shown in Fig.14. The low frequency voltage gain of the opamp is about 7760 and for an input swing with peak of 30μW, the output swing of the opamp reaches to 233mV.

The spectrum of the output waveform of the opamp is shown in Fig.15. The opamp has a very good linearity characteristics and the total harmonic distortions of the opamp is only 3% for ±233mV output swing. Such a high linearity is due to the source resistance R_s acting as the degeneration resistance and minimizing the harmonic distortions of each amplifier stage used in design of the two-stage opamp.

The common mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR) of the opamp are shown in **Error! Reference source not found.** (a) and (b). The CMRR has a corner frequency at 100GHz and the PSRR has a corner frequency at 1GHz. The CMRR achieves 40dB and the PSRR achieves 54dB signal rejection. The post layout characteristics of the opamp are listed in **Error! Reference source not found.**. The high performance of the SNT opamp indicates these transistors are good choices for future integration of high speed and low power mixed signal circuits.

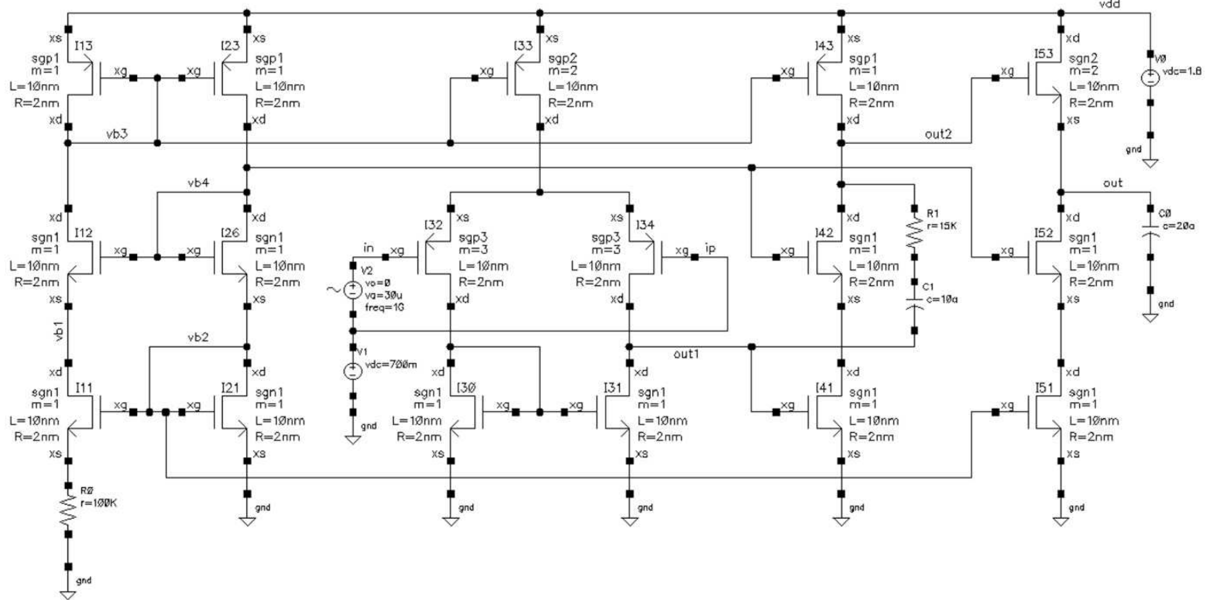

Fig. 9 The Schematic of Two-Stage Opamp

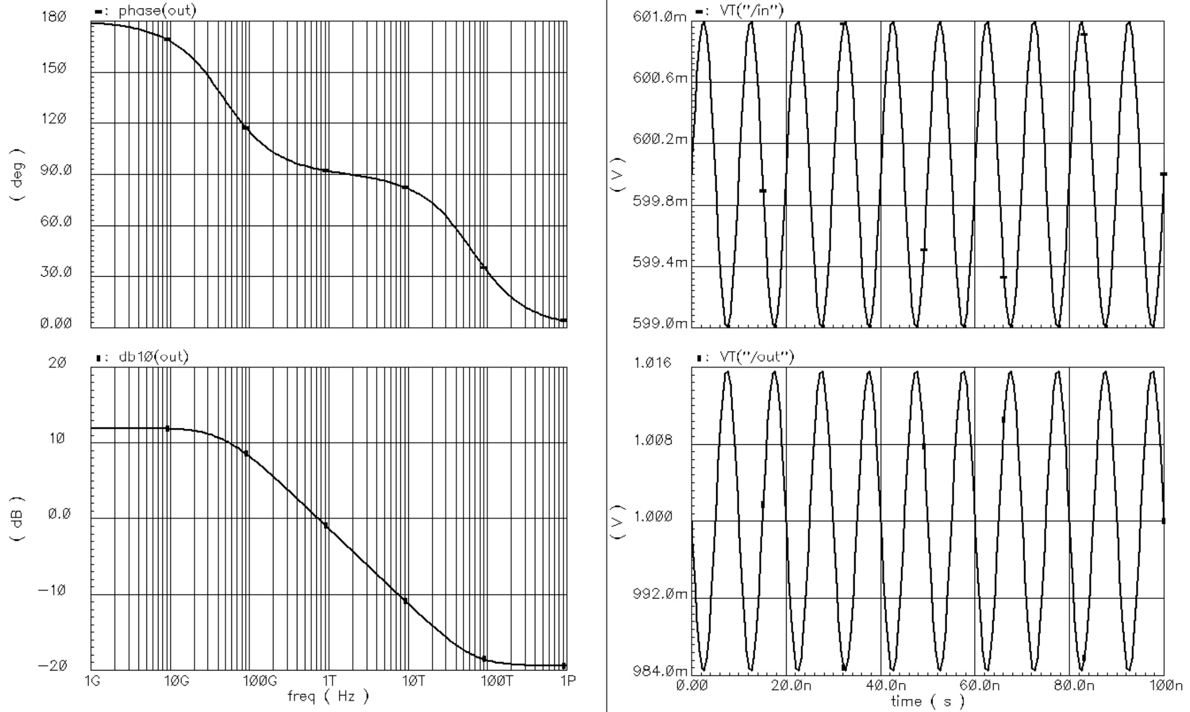

Fig.10 Frequency and Transient Responses of the Differential-Pair Amplifier

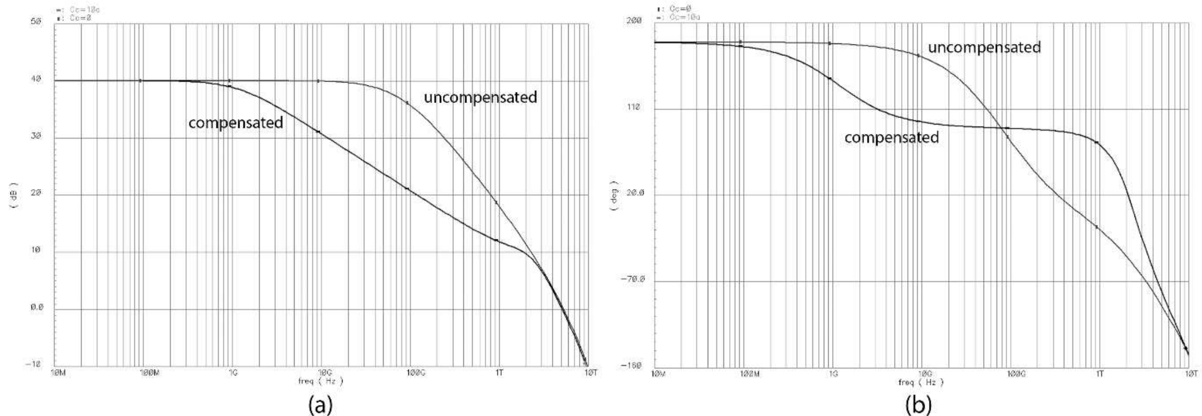

Fig.11 (a) Gain and (b) Phase Bode Plots of the Compensated and uncompensated Opamp

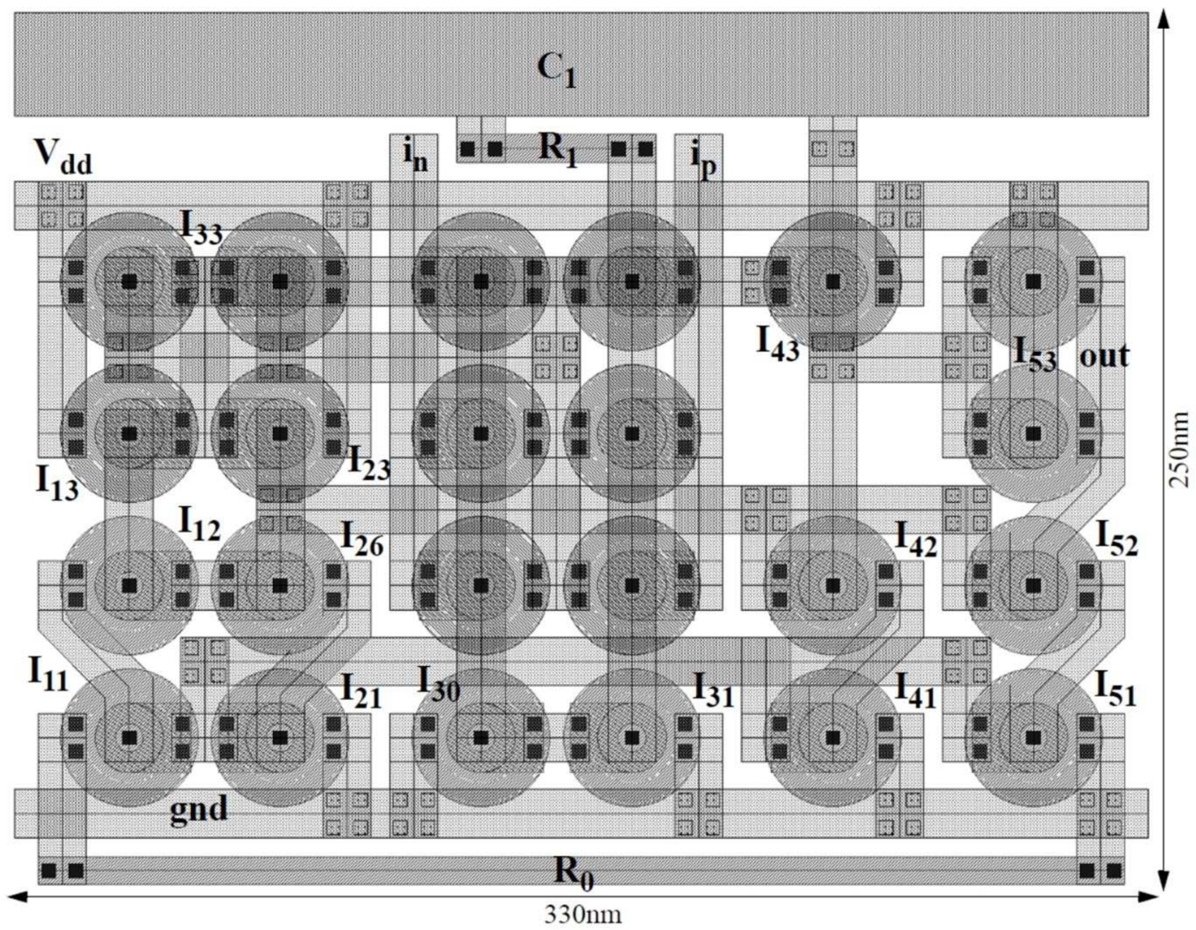

Fig.12 The Layout of the Two-Stage Opamp

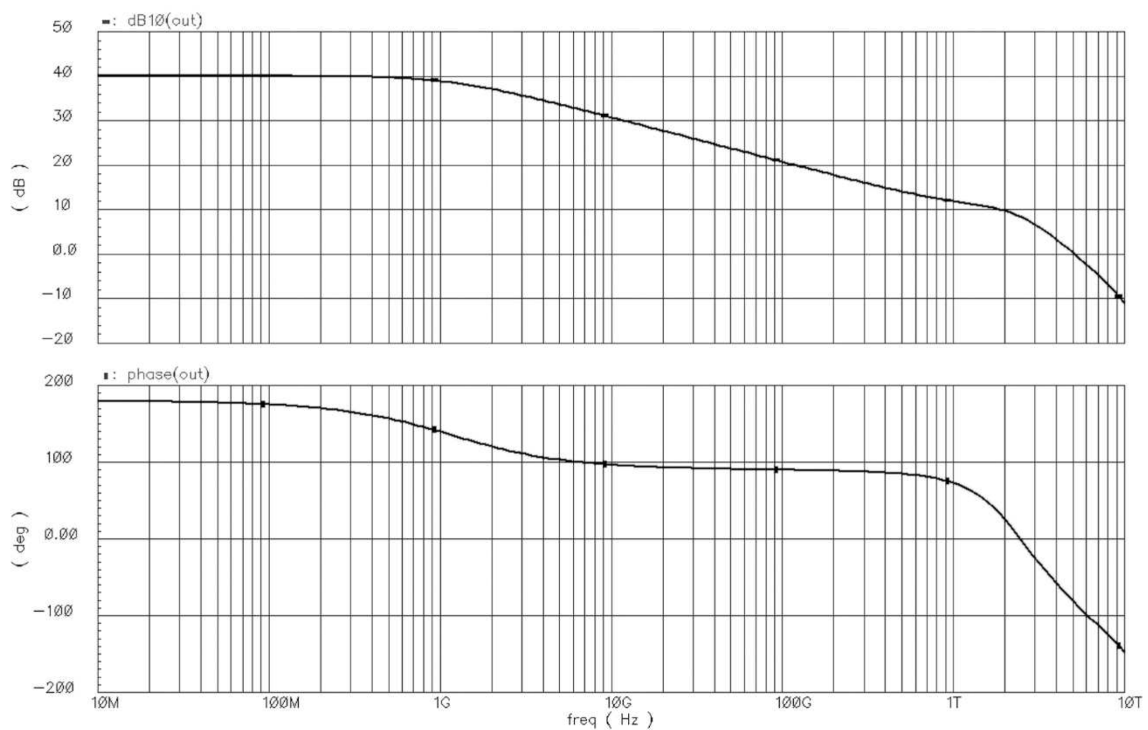

Fig.13 Frequency Response of the Two-Stage Opamp

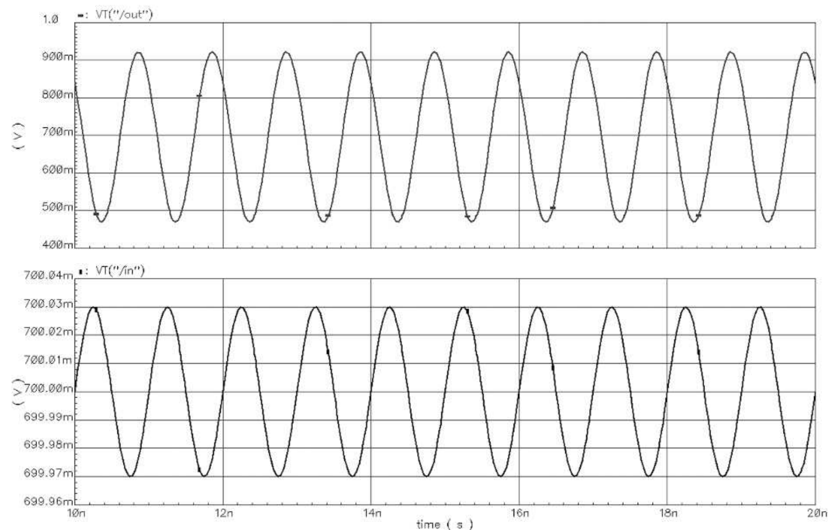

Fig.14 Transient Input and Output Waveforms of the Opamp

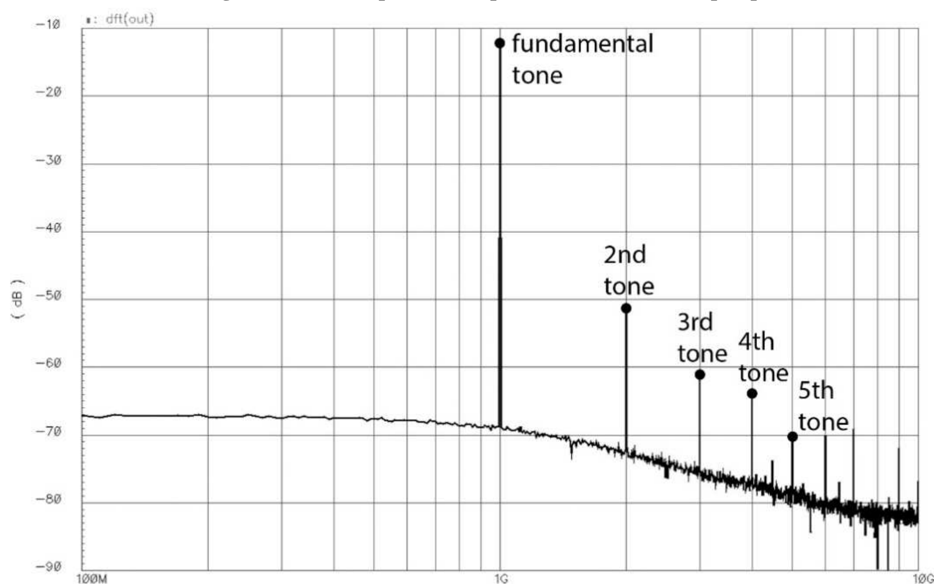

Fig. 15 The Spectrum of the Output Waveform of the Opamp

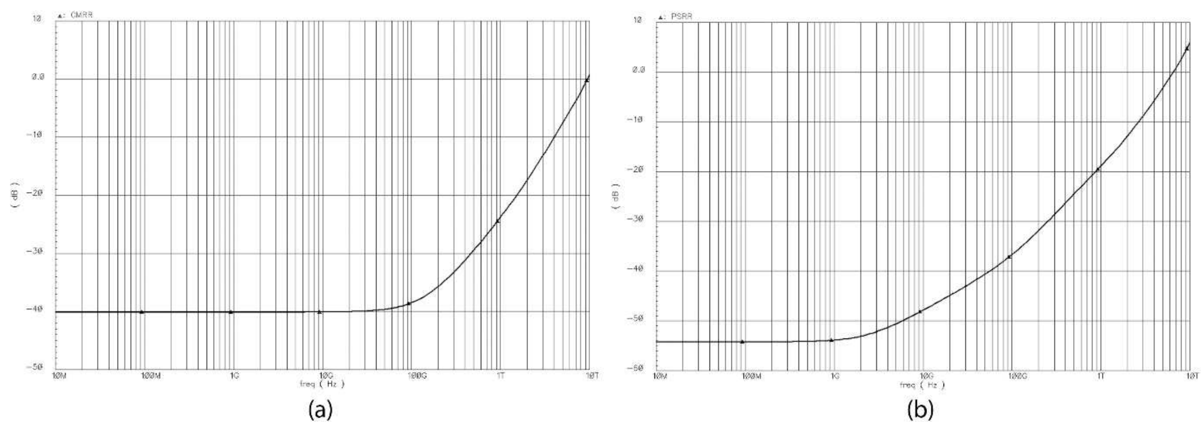

Fig.16 (a) CMRR and (b) PSRR of the Two-Stage Opamp

CONCLUSION

Design of a standard two-stage opamp using surrounding-gate nanowire transistors with 10nm channel length and 2nm channel radius was presented in this paper. The amplifier has an area of 320nm by 250nm. It operates from 1.8V supply and has a voltage gain of 40dB and a phase margin of 42°. The current gain cutoff frequency of the amplifier is 5.1THz. The common mode and power supply rejection ratios are 40dB and 54dB, respectively.

The opamp presented in this work provides a low-power and high-frequency performance suitable for applications such as internet of things and high speed wireless communications. Using nanowire transistors with surrounding gate structures is a suitable candidate for generating future VLSI technologies.

Table -1 Post layout Characteristics of the Two-Stage Opamp

Supply Voltage	1.8V
Biasing Circuit Power Dissipation	2.4μW
Opamp Circuit Power Dissipation	4.8μW
Maximum Output Linear Signal Swing	0.5V
Input DC Voltage Level	0.7V
Open Loop Voltage Gain (at 1 GHz)	7760 or 38.9dB
Open Loop Phase Margin (at 1 GHz)	42°
Open Loop Unity Voltage Gain Cutoff Frequency	5.1THz
Load Capacitor	20aF
Common Mode Rejection Ratio	40dB
Power Supply Rejection Ratio	54dB
Total Harmonic Distortion	3%
Slew Rate (High to Low)	-2V/ns
SLew Rate (Low to High)	2V/ns
Area	0.0825 μm2 or (330nm×250nm)

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