International Journal of
Intelligent Engineering & Systems

http://www.inass.org/

Portable data acquisition system based on FPGA and USB

Cao XiaoQiang,* Zhang Jun, Xiong Xing
School of Electronic Engineering
Tianjin University of Technology and Education
*Corresponding author's Email: ganono@163.com

Abstract: Nowadays, along with the development of technology of the high-speed Analog to Digital Converter (ADC) and Field Programmable Gate Array (FPGA), the design and the implementation of high-speed and high-accuracy data acquisition system is also becoming economic and feasible. In this paper, we designed a high-speed, high-precision, portable data acquisition and processing system in Altera Corporation cyclone II FPGA platform, and achieved the communication between the system and PC via USB2.0 interface. The whole system is divided into four parts: the A/D module, the FPGA module, the USB module and the LABVIEW (Laboratory Virtual Instrument Engineering Workbench) module. We used AD9467 as the core chip of the A/D module, and the characteristics and specific circuit design of AD9467 are explained in detail; the FPGA module is the core of the entire system, which is not only the center of the signal conditioning but also the control center to ensure the whole system to work in an orderly manner. We also introduced the concrete realization of the design of clock part, LVDS converter module and USB control module. The programming language used verilog hardware description language. And then we introduced the design of the USB module in detail where the Lab VIEW module was the module of human-computer interaction that introduced the concrete realization of the PC display software using G language. Finally, we debugged and tested the entire system, the results show that the design can work very well and meet the requirements of the system design.

Keywords: Data Acquisition, AD9467, FPGA, Verilog, USB, LabVIEW, G language.

1. Introduction

In modern times, data acquisition and processing technology have a wide range of applications to the fields of communication, aerospace, medical, radar, and weather. With the rapid growth of the importance of the data acquisition and processing system in the modern military and scientific research, the requirement of data acquisition and processing equipment is also rising. In high-speed and high-accuracy measurement such as signal measurement, picture processing and audio signal processing, high-performance data acquisition and processing is needed. What's more, technology is needed for high-speed, high-accuracy data acquisition and processing.

Nowadays, there are a lot of data acquisition systems, some are high-accuracy but not high-speed; some are high-speed but not high-accuracy. In this paper, we try to design a system to solve this problem. In addition, we apply the concept of portable data acquisition to the system, and use analog-to-digital converter AD9467 and high-speed USB as high conversion rate and high sampled accuracy device. The data acquisition system designed in the paper has characters of high rate, high accuracy, pulling and playing in any time at any place (if you carry a Personal Computer). This system has three core features:

- High speed: 250 MSPS conversion rate.
- High accuracy: 16-bit sampled accuracy.
- Potable: Its power comes from computer and it can work in any time at any place.
- Simple and quick Connection: All USB peripherals using common connector can connect to the computer simply and easily as the installation process is automated highly. We do not have to open the case or consider the allocation of resources. Without turning off the computer power supply, hot-plug can be realized.

2. The Overall Design of System

This system mainly consists of four parts: an A/D module, an FPGA module, a USB module and a LABVIEW module. The A/D module is data acquisition and then converts the acquired analog signal into digital signal. The main responsibility of FPGA module is processing the digital signal, including digital signal detection, calibration and control of other chip. The main responsibility of the USB module is transmitting the digital signal to the host computer using USB2.0 high-speed interface. The main responsibility of LABVIEW module is display of the man-machine interface. You can see the block diagram of the overall design of system in Figure 1.

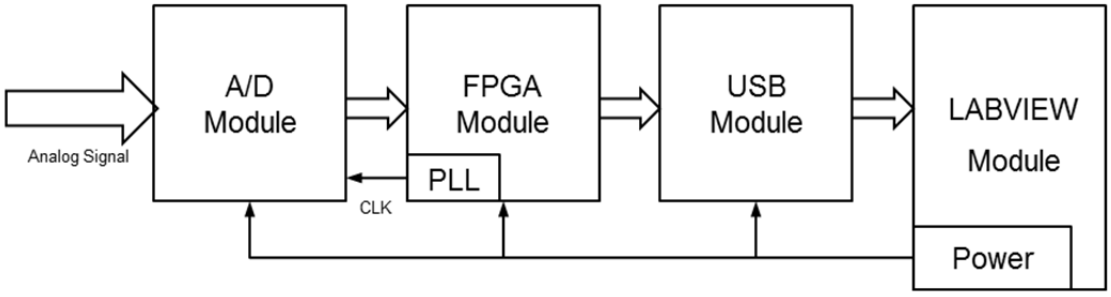

Figure 1 The structure block diagram

3. The A/D Module

3.1 Key features of AD9467

The A/D module is responsible for collecting analog data and it converts the analog data to a digital signal to feed to the subsequent processing module. Taking into account the low-power, high-speed and high-accuracy requirements, we selected an ADC chip of AD9467 of ANALOG DEVICES Corporation. The AD9467 is a monolithic and Intermediate Frequency (IF) sampling analog-to-digital converter (ADC). It is optimized for high performance over wide bandwidths and ease of use. Key features of AD9467:

◆ High speed: 250 MSPS conversion rate.

◆ High accuracy: 16-bit sampled accuracy.

◆ Ultra-low Power: The internal power-down feature supported via the SPI and typically consumes less than 5mW when disabled.

◆ Strong anti-jamming capability: Data outputs are LVDS compatible (ANSI-644 compatible), a low voltage differential input clock and include the means to reduce the overall current needed for short trace distances.

◆ Double voltage power supply: The ADC requires 1.8V and 3.3V power supplies for full performance operation.

◆ Optional features: Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

◆ Ease of use: On-chip reference, high input impedance buffer, adjustable analog input range, and an output clock to simplify data capture.

3.2 Schematics

3.2.1. Differential input schematic

There are several ways to drive the AD9467. For applications, the SNR and SFDR are key parameters. In this paper, using the ADL5562 differential drivers to drive the AD9467 provides an excellent and flexible gain option to interface to the ADC for both base- band and high IF applications, as shown in the schematic in Figure 2. Using an amplifier also provides better isolation from the preceding stages as well as better pass-band flatness. Performance plots of these amplifiers can also be seen in Figure 3.

3.2.2. Clock input schematic

For optimum performance, the sample clock inputting CLK+ and CLK- of AD9467 should be clocked with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK- pins via a transformer or capacitors. These pins are biased internally and require no additional biasing.

Figure 4 shows a schematic for clocking the AD9467. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock

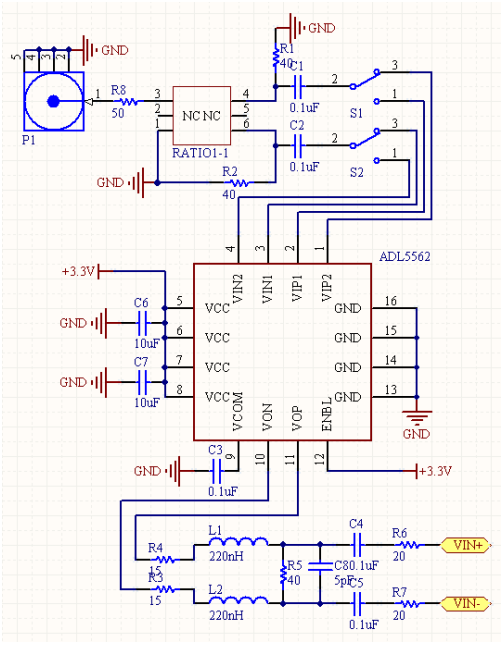

Figure 2 Wideband differential amplifier input circuit schematic using the ADL5562

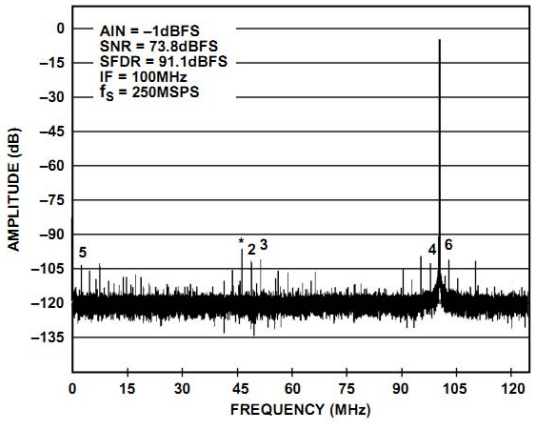

Figure 3 Single-tone FFT performance plot using the ADL5562 amplifier, gain = 6 dB, and the AD9467-250

excursions into the AD9467 to approximately 0.8 Vp-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9467, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

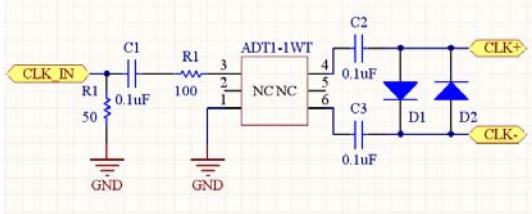

Figure 4 Transformer-coupled differential clock schematic

3.3 Caution

3.3.1. Digital output coding

It needs to be noted that, the chip is affected by the working voltage in practice and has some inherent error, so the output digital signal is not strictly 0 level, i.e. there may be a bias, when the VIN = 0V. This bias will have a huge impact on the subsequent power spectrum estimates. For example, when the AD9467 high-speed data acquisition module works in the following circumstances: AVDD1 = 1.8V, AVDD2 = 3.3V, AVDD3 = 1.8V, DRVDD = 1.8 V, the specified maximum sampling rate, 2.5V pp differential input, 1.25V internal reference, AIN = -1.0dBFS, DCS on, default SPI settings, unless otherwise noted. The sampling result of 0V is from 31,222 to 34,314, while the theoretical value should be 32768, so the bias is about 1546 points. The bias needs to be rectified by means of programming (sampling signal + /-1546). If we do not correct the bias, the system will generate a lot of low frequency and DC components that will drown the small sampling signal.

3.3.2. Power source

■ Separate analog power and digital power:

The stability of AD9467 power supply must be good. The AD9467 digital and analog power supplies should be separated to prevent high-speed digital output change from being coupled into the analog power switch current. A 0.01-0.1μF ceramic capacitor is placed as close as possible to the power to filter the wave of high-frequency and a paralleled 10μF tantalum capacitor to filter the low frequency noise.

4. The FPGA Module

This module includes the design of hardware and software. The specific design is in the following.

4.1 Hardware

In the design of hardware of this module, only designing a FPGA minimum system will be able to meet the requirements of this paper. There are about reset circuit, the external clock circuit, power supply circuit, JTAG and AS download interface and debug circuit and so on in the FPGA minimum system, which will no longer be introduced in this paper.

4.2 Software

The software design of FPGA mainly includes: the external input clock signal design of AD9467, the Software design of FPGA controlling USB interface device, and LVDS transmitter module.

4.2.1. AD9467 external input clock signal

FPGA chip's input signals include digital signal of 16 bits and one Synchronous clock signal, meanwhile FPGA needs to provide a clock signal of high frequency for ADC at the front. In order to provide clock signal for ADC, we use the PLLs (Phase-Locked Loop) of Quartus II.

The PLLs of Quartus II is also called The Flushbonading PLLs. Only in the FPGAs of Cyclone and Stratix PLLs is integrated. Altera Cyclone FPGAs, except that EP1C3 integrates one PLL, others integrate two PLLs. This kind of PLLs not only has superior performance, but also, according to needs, sets up the parameter, the phase shifting and the duty cycle of fractional frequency and frequency multiplication. There is an example of using PLL module to provide high clock signal to ADC, where it can change the value of the input clock signal of ADC only by changing some parameters, so it improves the flexibility of the system. The RTL diagram of PLL is shown in Figure 5.

Figure 5 The RTL diagram of PLL

The "inclk" is the clock signal of system, and its frequency is 50MHz. The PLL can set up the parameter of fractional frequency and multiplicate frequency and then put out. "clk_out" is output pin, providing clock signal for ADC where the parameter is 250MHz due to multiplicate frequency. The "rst" is a PLL reset pin. The "locked" is showing output clock and is stable after PLL processing active high. Functional simulation diagram is shown in the following Figure 6.

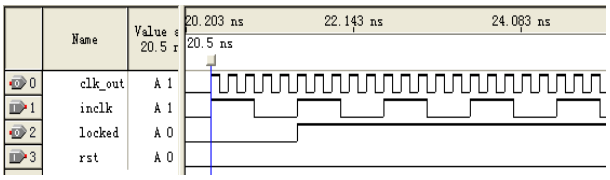

Figure 6 The timing simulation of PLL

4.2.2. LVDS transmitter module

The MegaWizard Plug-In Manager tool of Quartus II software offers IP for processing LVDS signal. In AD9467 chip, some LVDS share a single pin, such as D0 and D1, D2 and D3, -, D14 and D15. So we only set 8×2 bits LVDS input channels and 8 bits output signals. In order to separate D0, D2, D4,-, from D1, D3, D5,-. The "REG_8" module is added. Its function is shown in Table 1. When input clock signal "inclock" is up, put d_in [7:0] to assign d_out[7:0]. And when input clock signal "inclock" is down, put d_in[7:0] to assign d_out[15:8].

Table 1 Function of "REG_8" module

Inclock	Assigning
Up	d_out[7:0]<=d_in[7:0]
Down	d_out[15:8]<=d_in[7:0]

The RTL diagrams of LVDS transmitter module is shown Figure 7.

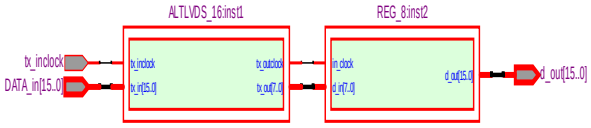

Figure 7 The RTL diagram of LVDS transmitter module

4.2.3. Software design of FPGA controlling USB interface device

We can see the connection block diagram of an EP2C8Q208C8N chip and a CY7C68013A-56PIN chip in Figure 8.

The CY7C68013A chip operates in slave FIFO mode and operates clock (IFCLK) supplied by external master.

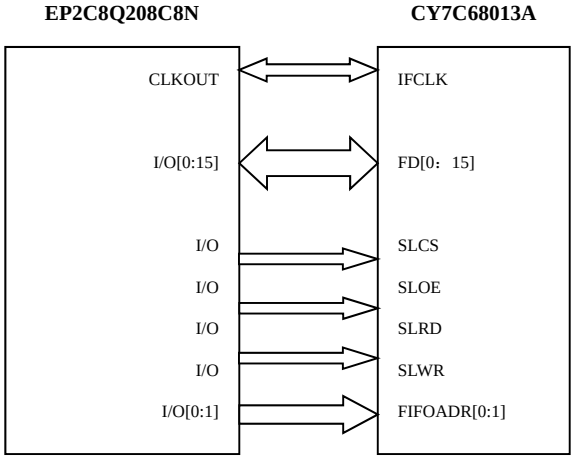

Figure 8 The connection block diagram

The chip slave FIFO architecture has eight 512-byte blocks in the endpoint RAM that directly serve as FIFO memories and are controlled by FIFO control signals (such as IFCLK, SLRD, SLWR, SLOE, PKTEND). SLOE, SLWE, SLRD, PKTEND signals are active low and controlled by external master FPGA.

When writing signals in the FIFO, we set SLOE=0, SLWR=0 and the rising edge of IFCLK. When read out signals from the FIFO, SLOE=0, PLTEND=0 and the rising edge of IFCLK. The software is too long, so it is not given in this paper.

5. The USB Module

In the design of USB module, the USB interface chip is CY7C68013A-56PIN of CYPRESS Corporation. The CY7C68013A-56PIN is a low price, strong function of high-speed Universal Serial Bus (USB) interface device.

5.1 Key features of CY7C68013A-56PIN

◆Single Chip Integrated USB 2.0 Transceiver, Smart SIE, Enhanced 8051 Microprocessor and Four Integrated FIFOs.

◆Ultra Low Power: I_{CC} No More than 85 mA in any mode.

◆ 8051 Code: Internal RAM is downloaded through USB.

◆8-Bit or 16-Bit External Data Interface.

5.2 Hardware

Figure 9 shows the external circuit schematic of CY7C68013A-56PIN which mainly includes: external clock circuit reset circuit and program storage circuit.

◆ There are usually two kinds of methods to provide clock signal for the CY7C68013A-56PIN chip:

One is to connect a crystal oscillator between XTALIN and XTALOUT of the CY7C68013A-56PIN chip; another method is to use one external clock source to connect directly to XTALIN pin, and XTALOUT pin is connected to none. This paper adopted the first method.

◆ EEPROM boot USB startups circuit:

EEPROM is used to boot the USB device, we only need to write the VID and PID of USB device to the EEPROM chip and connect EEPROM chip to the I^2C bus of the USB chip. 24LC256, with I^2C serial bus interface, is EEPROM chip of MICROCHIP Company. A0-A2 are address input pins. SCL and SDA are I^2C bus serial clock pin and serial address pin. WP is writing-protect pin. When WP is high, we can only read data from the device for the protection of the hardware data. When WP is low, we can not only read data but also write data from the device. All the 24LC256 operations follow the I^2C serial bus operation timing.

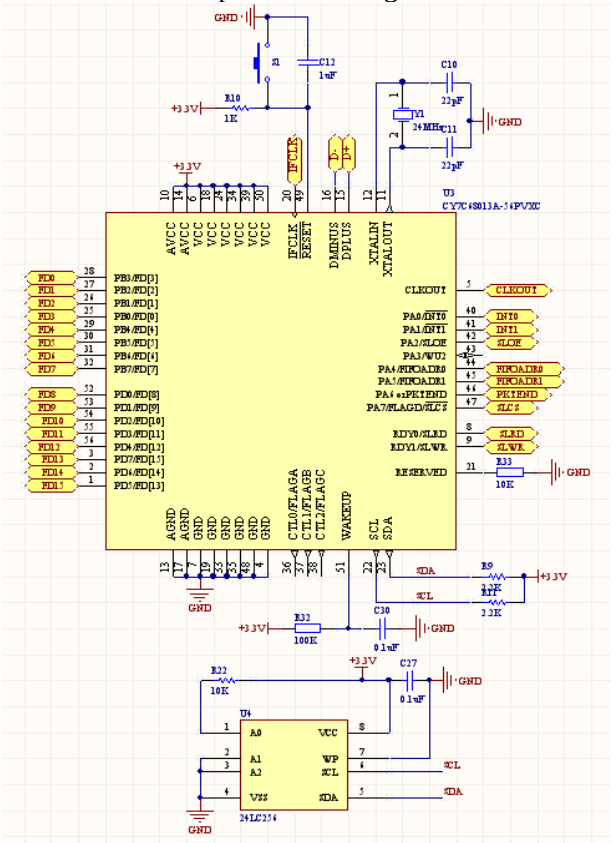

Figure 9 The external circuit schematic of CY7C68013A-56PIN

5.3 Software

The USB module software design consists of two parts, of which one is the firmware program of USB chip, and the other is the drivers of USB host computer.

The USB firmware program is a program written into EROM or EPROM (programmable read-only memory). It is a program code cured in the USB chip and it is responsible for the control and coordination of the USB chip for the completion of the agreement dealing with the recognition of the USB device, relisted, the data communication between the device requests and USB peripherals with USB host computer. USB driver is the configuration file based on the operating system. It is a small piece of code added to the operating system which contains information about the hardware. When you install new hardware, the driver is an essential component. If you do not have

a driver, the computer hardware will not work. With this information in the driver, the computer can communicate with the device. Host application communicates through the client driver and system USBI (USB Device Interface), and the collected data stream is processed according to the requirements needed based on Windows program. Figure 10 is the development diagram of USB software.

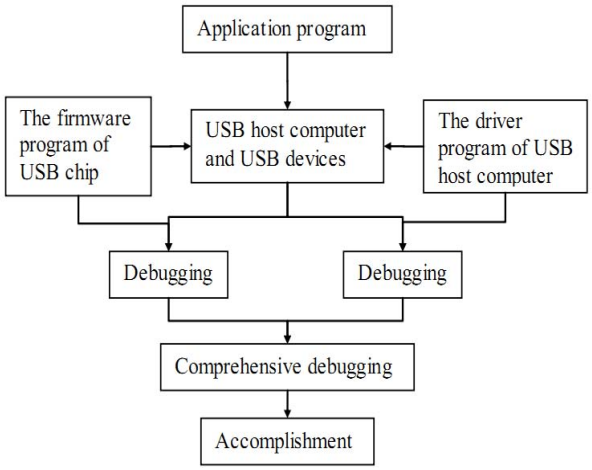

Figure 10 The block diagram of software development

5.3.1. Firmware program

For the firmware programming of USB chip, you can write it on the basis of chip resources. Cypress Corporation provides a development kit (CY3684 EZ-USB FX2LP Development Kit) for the most widely used EZ-USB chip. The development kit includes a typical firmware code; users can use it directly for developing and debugging the USB devices without any modification.

5.3.2. Driver software

The host computer uses the LabVIEW development platform, so the development of the driver program of this part needs to use NI-VISA development platform. This section is introduced in LabVIEW module.

6. The LabVIEW Module

In order to accelerate the development of the entire system, we choose to use the graphical programming software LabVIEW.

6.1 The main Advantages of LabVIEW

◆Easy to learn and use: It adopts graphical programming method (G Language) and provides a rich graphical control and engineers. If the users do not quite understand C language, B language Java or other text programmable languages, they can still easily use LabVIEW.

◆Real-time compiler: The compiler built-in can complete the compilation automatically when users write program. Therefore if there is any syntax error when users write program, the error will be displayed immediately.

◆By using the application builder we can publish EXE, dynamic link library, or the installation package easily.

◆Mixed programming: By using the technology of DLL, CIN node, ActiveX, NET or MATLAB script node, mixed programming can be achieved easily using LabVIEW and other programming languages.

◆Easy to communicate: LabVIEW provides a lot of drive and special tools, so it can connect and communicate with almost any interface with any interface.

◆ Powerful signal analysis and processing capacity: LabVIEW contains more than 600 analysis functions for data analysis and signal processing.

◆Strong scalability: NI provides a number of add-on modules for the applications of LabVIEW in different areas such as real-time module, PID module, FPGA module, Data logging and DSC module, machine vision module and touch screen module.

6.2 NI-VISA

The LabVIEW can control the USB device that it can identify, so LabVIEW needs to be installed with specific drivers program (NI-VISA). NI-VISA is virtual instrument software that can connect USB devices and LabVIEW easily.

Configure the NI-VISA:

Firstly, NI-VISA should have been installed on the computer before the USB device is connected. You should not install the USB device driver. We need three steps to configure the USB device in order to use the NI-VISA to control it:

1. Using DDW (Driver Development Wizard) to create an INF document.
2. Installing INF document and connecting USB devices that use INF documents.
3. Using the NI-VISA Interactive Control tool to test equipment.

The specific configuration is omitted in this paper.

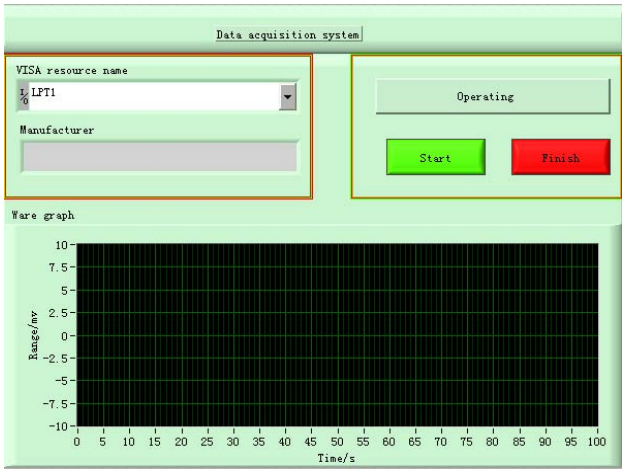

Figure 11 The main interface of the system

6.3 The software implementation of host computer

In the system, we use a sequence structure to complete the design of the various sub-VI programs, and make it into a single module. Of course, each module is composed of smaller modules, so that not only the readability is enhanced, programming complexity is reduced, but also it is easy to maintain to make the block diagram clearer and at the same time, avoid a lot of repeat programming. Figure 11 is the main interface of the system.

7. Design of Supply Power

The power system is the core of the entire hardware system whose performance is critical to the entire system. In this section we focus on the design of the power supply circuit.

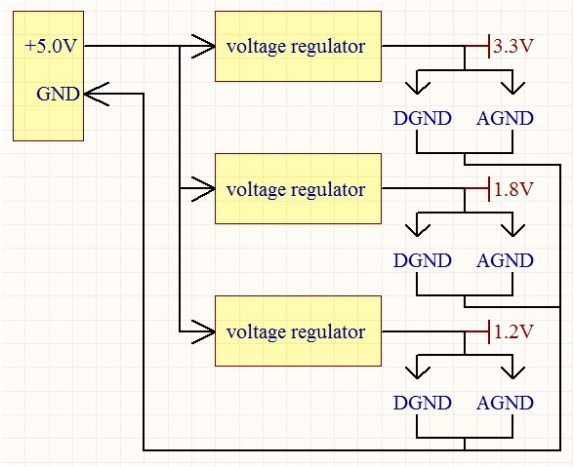

Figure 12 The block diagram of power supply

7.1 The overall design of power supply

In the hardware circuit of the system, the supply voltage of AD9467 chip is 1.8V and 3.3V; the supply voltage of the FPGA chip EP2C8Q208C8N is 1.2V and 3.3V; the supply voltage of the CY7C68013A is 3.3V. The external supply voltage can be obtained from the USB interface of PC, the voltage of the USB interface is 5V, so we need voltage regulators, the block diagram of the design is shown in Figure 12.

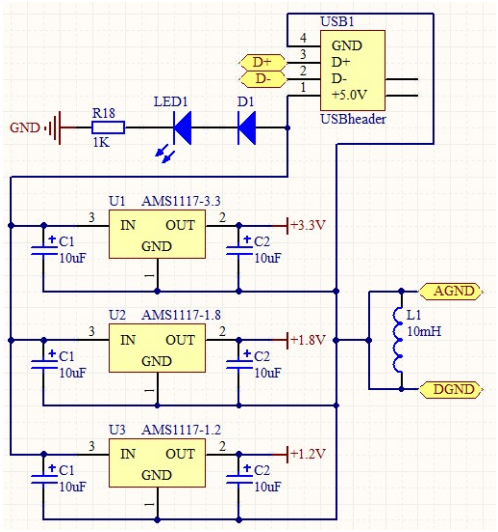

Figure 13 Power circuit schematic

7.2 Hardware circuit schematic

In the design of power circuit, we use the voltage regulators of AMS1117 series. The AMS1117 series of adjustable and fixed voltage regulators can provide 1A output current, so it is ideal for battery-powered systems. Figure 13 is a power hardware circuit schematic. AD9467, EP2C8Q208C8N and CY7C68013A have analog and digital ground, so in the power system we use the 10mH inductor to isolate the digital and analog ground, so that we can ensure the stable work of the chips and chips can work in the best condition.

7.3 Feasibility analysis

AMS1117 mainly provides electrical power for AD9467, EP2C8Q208C8N and CY7C68013A chips, as long as the AMS1117 output power is greater than power consumption of the AD946, EP2C8Q208C8N and CY7C68013A.

The output current of AMS1117 can be up to 1A.When the output voltage is 1.2V, the minimum value of the output power (P0) can be up to 1.2W. As the maximum power consumption (P1) of

AD9467 is 5mW; the maximum supply current of CY7C68013A is 85mA; the maximum power consumption (P2) is 280.5mW, therefore when working at the highest frequency, the power consumption of EP2C8Q208C8N (P3) is lower than 500mW. We can know: P0 > P1 + P2 + P3, so the design of power supply is feasible.

8. Test and Verify

In this paper, the hardware design is mainly divided into two parts, of which one part is the analog signal acquisition, and the other part is the digital signal processing. Therefore, the test can be divided into analog signal acquisition test and digital signal processing test. Here are the follows.

In the Analog signal acquisition test, we use the Quartus II SignalTap II Logic Analyzer tool.

◇AD9467 test:

Data outputs of AD9467 are LVDS compatible (ANSI-644 compatible), the purposes of debugging is transforming the LVDS signals into a standard binary code, and then, comparing it with the standard binary code of the ideal state in order to find the error value. Table 2 is the comparison table of measured output data signals and the ideal output signals. In this table, we only give five voltage contrasts.

Description:

※AD9467 the valid bit is 14 bits, the highest bit is invalid and the second highest bit is the sign bit.

※Input frequency of AD9467 is 50MHz.

※The analog input signal is a sine wave whose frequency is 1MHz and the lowest voltage is 0V.

Note: of course, when the waveform and frequency of the input signal is different, the error value may be different. Even with the same waveform and the same frequency, the measurement value may be different in different time.

Table 2 The comparison table

The highest voltage	The value of ideal wave peak	The value of measured wave peak	The error value (decimal)
0v	00 0000 0000 0000	00 0100 0000 0011	3
0.5v	00 0000 1111 1111	00 0001 0000 1010	11
1v	00 0001 1111 1111	00 0010 0000 0001	2
1.5v	00 0010 1111 1111	00 0010 1011 1010	69
2v	00 0011 1111 1111	00 0011 1100 0101	58

When the input sine wave signals are set as follows: frequency is 3MHz, peak-to-peak voltage is 2v and trough voltage is 0V, the measured waveform is shown in Figure 14. In the drawings, d_adc is data output bits of AD9467; d_fpga is the digital signal after FPGA processing; clk_adc is input clock (50MHz) of AD9467. There are 20 clk_adc clock rising edges between two black bars. The output sine wave frequency can be calculated as 50/20 (MHz), consistent with the input frequency to meet the design requirements.

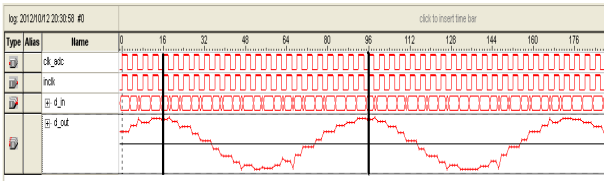

Figure 14 The measured waveform

◇Spectrum analysis test：

Take sine wave for example, the set of signal source parameter is shown in Table 3. When the sampling rate is 10 MHz, the spectrum analysis diagram of sampled digital data is shown in Figure 15.

Table 3 Signal source parameter

Parameter	Value
Output frequency(f_s)	1MHz
High voltage(V_H)	+1v
Low voltage(V_L)	-1.5v

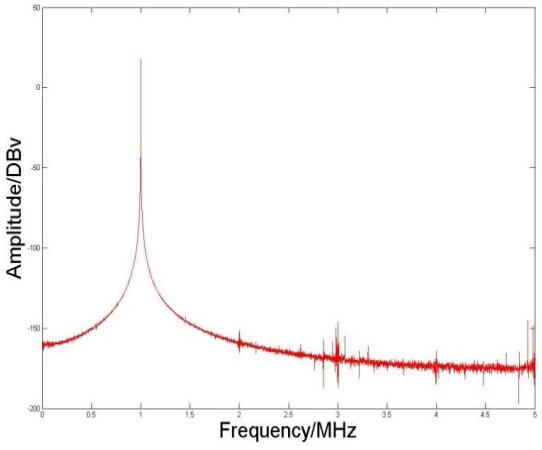

Figure 15 Spectrum analysis diagram

9. Conclusions

This paper designed a high-speed, high-accuracy and portable data acquisition system based on FPGA and USB. Without adding extra power, we acquire electricity directly from USB interface. Experiments show that the system can convert the digital signal to the host computer. The entire system is designed to be simple, stable. So it reaches the design requirements. The data acquisition board is shown in Figure 16.

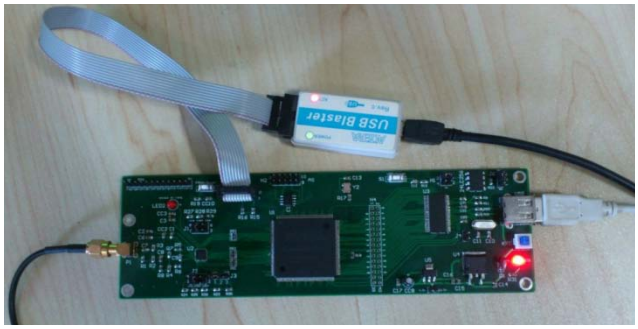

Figure 16 Data acquisition board

Acknowledgments

This work is supported by the National Science Foundation of China (grants 61071204) and the Development Foundation of Tianjin University of Technology and Education (grants KJY11-3).

References

[1] ALTERA Corporation, *Cyclone II Device Handbook*, Volume 1.2007.

[2] Liu XiaoHui, *The Frequency-Shift Keying Signal Demodulation Research on LabVIEW*, 2009.

[3] Cypress Semiconductor Corporation, *Cypress EZ-USB FX2 high-speed USB Interface Device*, 2002.

[4] Luo XiangDong, *Design of USB Interface Based on FPGA and CY7C68013A*, 2010.

[5] Analog Devices, *AD9247: Complete Data Sheet [Z]*, 2011.

[6] BorghiT, BonfantiA, Zambra G and Gusmeroli R, *A ComPact Multichannel System for Acquisition and Processing of Neural Signals*, Proeeedings of the 29th Annual Intemational Conference of the IEEE EMBS Cite Intemational, August23-26, 2007:441-444.

[7] Leong, C., Bento, P., Lousa，P., Rego, J., Rodrigues and P.Silva, *Teixeira,Design and test issues of an FPGA based data acquisition System for medical imaging using PEM*, Vol.53, No.1, June, 2006.

[8] Leong, C., Bento, P. and Rodrigues, *Design and test issues of a FPGA based data acquisition system for medical imaging using PEM*, Real Time Conferenee, 2005.14th IEEE-NPSS, No. 10 June, 2005.

[9] B.Murovec, S., and Kocijancic, *Edueational data aequisition system with USB interfaee*, IEEE.2003.

[10] Yu Zheng, *Detailed explanation of power integrity design*, 2009.

[11] Wang Yue, Zhang Xiaolin and Li Huaizhou, *Study on high-speed and large capacity recorder of radar video echo signal*, Communication Software and Networks(ICCSN), 2011.

[12] B.Murovec, S., and Kocijancic, *Educational data acquisition system with USB interface*, IEEE. 2003.

[13] Nationnal Instruments, *LabVIEW Fundamentals*, August,2005

[14] Hegyesi and Imrek, *Development of an FPGA-based data acquisition module forsmall animal PET*，Vol. 5, No. 22 Oct, 2004.

[15] Yonghai Ning, Zongqiang Guo, Sen Shen and Bo Peng, *Design of Data Acquisition and Storage System Based on the FPGA*, Procedia Engineering, 2012.

[16] Zhou Wenjie, Zhao Jing, and Zhao Li, *ARMS and Linux-based FPGA-driven design* [J], new and special device applications, 2010. (In Chinese).

[17] R.Jama，L.Wenzel, *The applicability of the visual programming language LabVIEW to large real-world applications*, 11th international IEEE Symposium on Visual Languages，2002,45-47.

[18] Asan Ganl, M.J.E.Aalami, *A LabVIEW based Data Acquisition System for Vibration Monitoring and Analysis*, IEEE Design and Test of Computor,2002，Page(s): 62-74.