DESIGN AND ANALYSIS OF 4:1 MULTIPLEXER USING AN EFFICIENT REVERSIBLE LOGIC IN 180nm

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Abstract:-

Multiplexer's square measure is a typical building block for data-paths, and is used extensively in a variety of applications together with the processors. In this paper authors have proposed a 4:1 multiplexer using PFAL and ECRL adiabatic logic design technique and compared with the Conventional CMOS Multiplexer. The basic approaches that we used for reducing energy/power dissipation in conventional CMOS circuits include varying the rise time and full time, on decreasing frequency and minimize the switching activities with efficient charge recovery logic. The Adiabatic switching technique based upon the energy recovery principle is one of the techniques which is widely used to achieve low power VLSI design circuits. In the following paper, the power dissipation of various adiabatic circuits is calculated and then simulated using TANNER tool.

***Keywords*:**Adiabatic,ECRL,PFAL,T-SPICE, 4:1 Multiplexer Using ECRL and PFAL.

1. Introduction

Multiplexer is an important part in implementation of signal control systems and memory circuits. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A Multiplexer in also called the data selector **[1].** The low power consumption is one of the foremost vital problems within the system SOC design completely different techniques and technologies for low-power design in high-speed interface applications square measure developed and Conjointly applied within the sensible designs **[2].** There are numerous ways in which the square the measure is widely used for reducing the facility dissipation in circuits by reducing the change activities, offer voltage and load capacitances. These ways solely try and minimize the facility dissipation. In this paper, we present the design of 4:1 multiplexer using adiabatic logic and compare with conventional CMOS.

1.1 Adiabatic Principle

The word ADIABATIC emanates from a Greek word that is utilized to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In authentic-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by decelerating the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as ENERGY RECOVERY CMOS. In the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems. Here, the load capacitance is charged by a constant-current source (instead of the constant-voltage source as in the conventional CMOS circuits). Here, R is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp **[3].** Assume, the capacitor voltage VC is zero initially.

The voltage across the switch = IR 1

P(t) in the switch $=I^2R$ 2

Energy during charge $= (I^2R)T$

E $E=(I^2R)T=(CV/T)^2 RT = C^2V^2/T\ R$ 3

$E = Edis = (RC/T)CV^2 = (2RC/T)\ (1/2CV^2)$ 4

where, the various terms of Equation (3) are described as follows:

E — energy dissipated during charging,

Q — charge being transferred to the load,

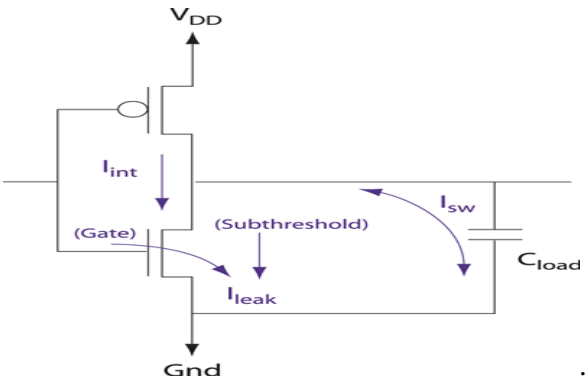
C — value of the load capacitance,

R — resistance of the MOS switch turned on,

V — final value of the voltage at the load,

*T*_ time .

Now, a number of observations can be made based on Equation (3) as follows:



"Figure.1:Adiabatic CMOS Inverter."

(i) The dissipated energy is smaller than for the conventional case, if the charging time T is larger than 2RC. That is, the dissipated energy can be made arbitrarily small by increasing the charging time,

(ii) Also, the dissipated energy is proportional to R, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on-resistance of the PMOS network will reduce the energy dissipation.

1.1.1. Adiabatic logic structures are mainly of two types:

1. Partially adiabatic logic. They are classified as –

i) Efficient charge recovery logic (ECRL)

ii) Quasi Adiabatic Logic(QAL)

iii) Positive feedback adiabatic logic (PFAL)

iv) 2N-2N2PLogic

v) True single phase adiabatic logic (TSAL)

2.Fully adiabatic logic. They are classified as

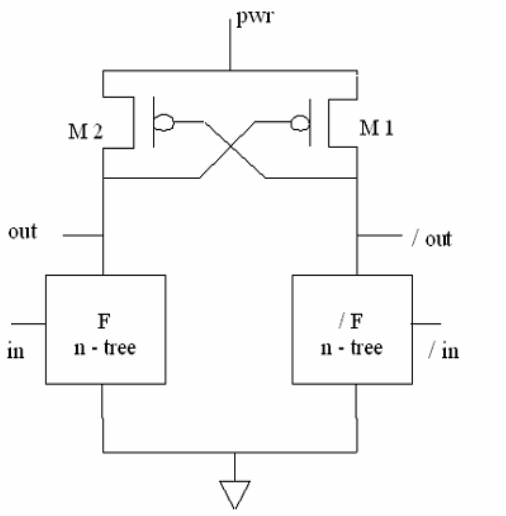
i) Pass transistor adiabatic logic

ii) 2 Phase adiabatic Static CMOS logic (2PASCL)

iii) Split rail charge recovery logic (SCRL)**[4].**

1.1.2. ECRL Technology

ECRL technology is that in which precharge and evaluation simultaneously performed and by implementing this method energy dissipation is reduced to a large extent. ECRL eliminates the precharge diode which dissipates less energy than the other adiabatic methods. It can also eliminates the need of more number of PMOS switches, in ECRL only two PMOS switches are used and it is the matter of fact that PMOS is the big source of power dissipation. It provides the charge on the output with full swing and it charges the load capacitance with the constant supply which is completely independent of the input signal **[5].**



"Figure2: ECRL Logic Circuit."

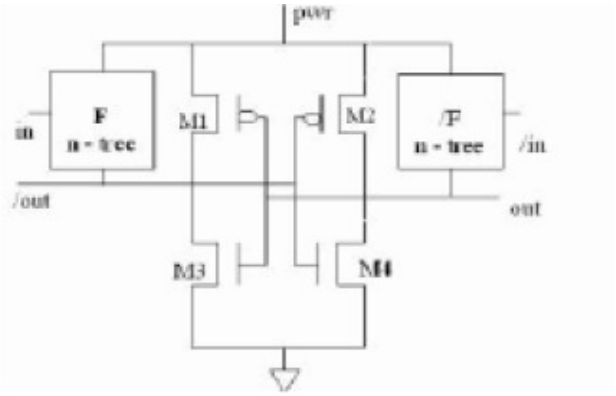
The circuit has two cross coupled transistors M1 and M2 of PMOS and two NMOS functional blocks for ECRL adiabatic logic implementation. An AC power supply pwr is used, so as to recover and reuse the supplied energy. Both out and /out are drive a constant load capacitance independent

of the input signal. The cross coupled PMOS transistors helps for obtaining full swing in both

precharge and recover phases. ECRL always provides the charge on the output with the full swing. Hence, the voltage on the supply clock approaches to |Vtp|, the PMOS transistor gets turned off**[6].**

1.1.3. PFAL Technology

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery **[7].** The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS M1-M2 and two NMOS M3-M4, that avoids a logic level degradation on the output nodes out and /out. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs**[8].**



"Figure3:PFAL Logic Circuit."

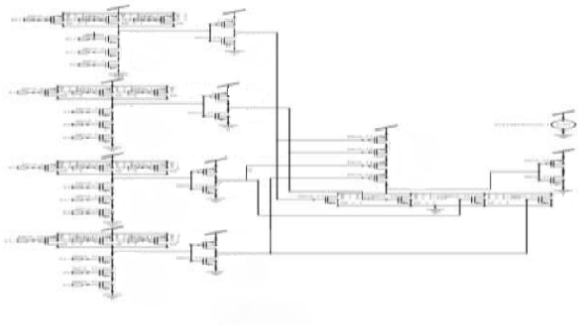
Thus the equivalent resistance is smaller when the capacitance needs to be charged.

2. Logic design styles

Multiplexer circuit:

2.1.1:4:1 multiplexer using Conventional CMOS:

A Multiplexer sends one of 2n input lines to a single output line. A Multiplexer has four sets of input X (0), X (1), X (2), X (3) and two select lines S (0) and S (1). The Multiplexer output is in a single bit Y**[9].**

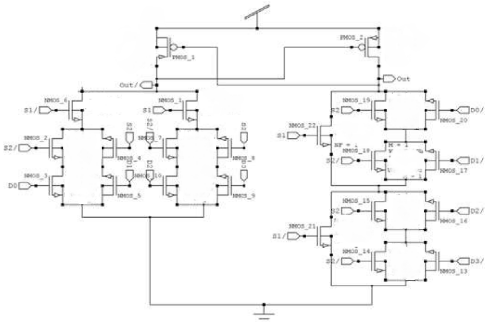


"Figure4:.4:1Mux using conventional CMOS."

2.1.2:4:1 multiplexer using ECRL logic:

Input in is at high and in b is at low. At the beginning of a cycle, when the supply clock „pwr" rises from zero to VDD , out remains at a ground level, because in turns on F- tree (NMOS logic tree). /out follows pwr through M1. When pwr reaches VDD, the outputs hold valid logic levels. These values are maintained during the hold phase and used as inputs for the evaluation of the next stage. After the hold phase, pwr falls down to a ground level, /out node returns its energy to pwr so that the delivered charge is recovered. Thus, the clock pwr acts as both a clock and power supply[10].

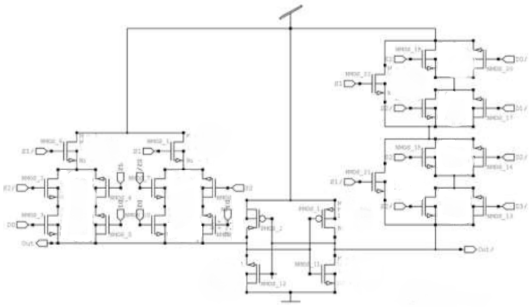
4*1 Multiplexer having inputs(D0,D1,D2 and D3) along with select lines(S1 and S2), we get the output Y.



"Figure5:.4:1 Mux Using ECRL Logic."

2.1.3:4:1 Multiplexer using PFAL:

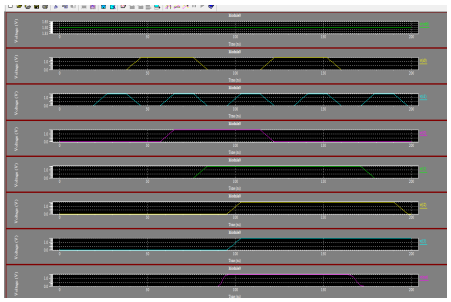
The structure of Positive Feedback Adiabatic Logic PFAL where two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETs, rather than by only two PMOSFETs as in ECRL, and that the functional blocks are in parallel with the transmission PMOSFETs [11]. Thus the equivalent resistance is smaller when the capacitance needs to be charged. The ratio between the energy needed in a cycle and the dissipated one can be seen in figure 6. During the recovery phase, the loaded capacitance gives back energy to the power supply and the supplied energy decreases. The partial energy recovery circuit structure so called Positive Feedback Adiabatic Logic (PFAL) , has good robustness against technological parameter variations. It is a dual rail circuit[12].



"Figure6:.4:1 Mux Using PFAL Logic."

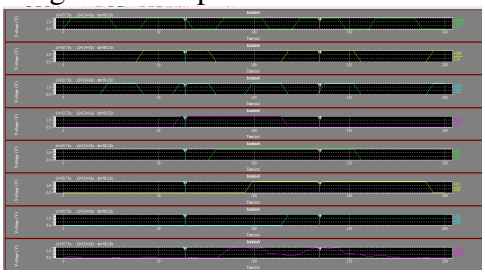
3. Simulation Results

In this paper different logic styles, ECRL and PFAL logic were used to design 4:1 Multiplexer. This 4:1 multiplexer was design on s-edit of tanner tool on 180nm technology. Figures shows schematics of multiplexers designed using three logic styles.



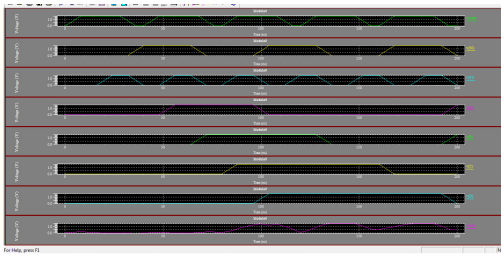
"Figure7:Simulation results Of 4:1Mux Using Conventional CMOS."

Figure 7 shows the simulated waveforms of 4:1 multiplexer using Conventional CMOS,where the bottom one signal indicate output while the top seven signals are inputs.



"Figure8:Simulation results Of 4:1Mux Using ECRL."

Figure 8 shows the simulated waveforms of 4:1 multiplexer using ECRL, where the bottom one signal indicates output while the top seven signals are inputs.



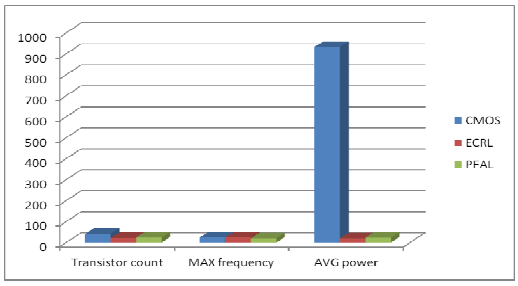
"Figure9:Simulation results Of 4:1Mux Using PFAL."

Figure 9 shows the simulated waveforms of 4:1 multiplexer using PFAL,where the bottom one signal indicate output while the top seven signals are inputs.

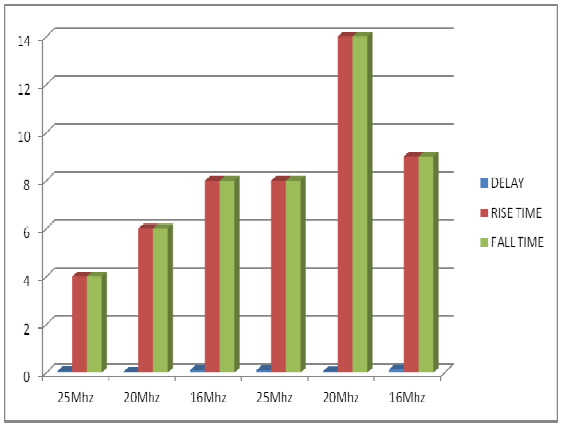
4. CALCULATION OF SIMULATION RESULTS OF 4:1 MULTIPLEXER

This section deals with the comparison of the CMOS logic style with the adiabatic logic style in terms of the average dynamic power dissipation,

rise time and fall time. This 4:1 multiplexer was simulated on tanner tool in 180nm technology.

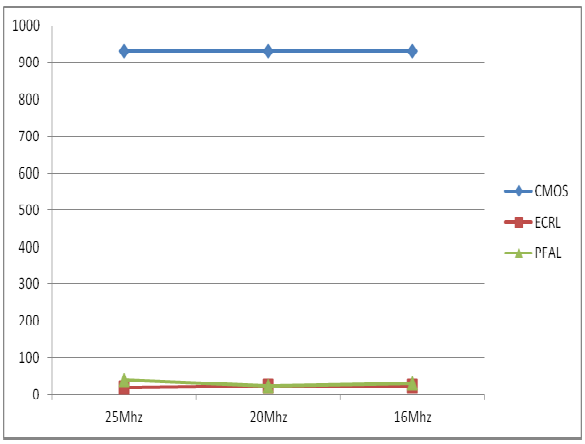


"Figure 10:Graph For Transistor Count,MAX Frequency and Average Power For 4:1 Multiplexer."



"Figure 11:Graph For Delay,Rise Time and Fall Time For 4:1 Multiplexer(ECRL and PFAL)."

FREQUENCY	4:1MUX (CMOS)	4:1MUX (ECRL)	4:1MUX (PFAL)
16 MHZ	932uw	23.65uw	31.76uw
20 MHZ	932uw	23.35uw	23.25 uw
25 MHZ	932uw	20.06uw	40.24uw



"Figure12:Avg. power verse Frequency For 4:1 Multiplexer."

"Table1: Power dissipation results for various circuits with frequency."

Table 1 shows power dissipation of adiabatic circuits and conventional circuit. It shows the dissipation in adiabatic circuit is less compared to conventional circuits.

"Table2: Average power dissipated, ax. Frequency, transistor count of cmos family and adiabatic ECR and PFAL family for 4:1 multiplexer."

Table 2 shows the comparison of CMOS, ECRL and PFAL in terms of transistor count, max. Frequency and average power dissipated.

Parameters	CMOS	ECRL	PFAL
Transistor count	42	22	24
MAX frequency	25Mhz	25Mhz	20Mhz
AVG power	932uw	20.06uw	23.25uw

"Table3: Delay,rise time and fall time of cmos family and adiabatic ecrl and pfal family for four- to- one multiplexer for different power clockfrequencies."

Table 3 shows the parameters like delay,rise time and fall time which are used in simulation.

16Mhz	**0.14**	**9**	**9**

Conclusion:

Authors have implemented the 4:1 multiplexer design with adiabatic and conventional CMOS and are compared with each other.A power reduction of 23.25 uw in PFAL ,20uw in ECRL compare with 932uw in conventional CMOS.. All the parameters are computed on Tanner Tool at 180 nm Technology at 1.5V supply voltage. This reduction technique can be used in applications such as Memory Designing, in high performance low power circuits and various high end processors.

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Parameters	DELAY	RISE TIME	FALL TIME
25Mhz	**0.07**	**4**	**4**
20Mhz	**0.04**	**6**	**6**
16Mhz	**0.11**	**8**	**8**
25Mhz	**0.1**	**8**	**8**
20Mhz	**0.06**	**14**	**14**
16Mhz	**0.14**	**9**	**9**