L-Z Source based Diode Clamped MLI for multilevel generation

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ABSTRACT

Multilevel inverters (MLI) have the capability of producing less distorted ac voltages across its output terminals. The output available across any MLI is a stepped sine wave. Among the available configurations diode clamped topology has the ability of providing reverse recovery ability for the switches. So in this project a new converter topology based on Z-Source configuration combined with a diode clamped multilevel is proposed. Usually classical Z-Source inverters contain a diode, capacitors and inductors for boosting the voltage. The Z-Source inverters suffer with inrush currents and resonance. The disadvantages of these capacitors are eliminated with the help of a new circuit comprising of inductors and diodes. The Z-Source of the network contains only inductors. The Z-Source acts like a current source and is cascaded with a diode clamped multilevel inverter. The main advantage of this configuration is that size of the filter is minimized and has the ability of producing least distortion in output current when the system is operated with lagging power factor loads. The proposed circuit is modelled and simulated using MATLAB. Total harmonic distortion levels are estimated with and without filters when supplying resistive and combination of resistive and inductive loads.

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I. INTRODUCTION

In recent years, various Z-source inverter (ZSI) topologies have been presented in numerous diversified studies. Some of the studies are focused on applications, modeling, controls, and modulation strategies, whereas others are focused on the development of new topologies. The ZSIs accomplish a single-stage power conversion with buck-boost capabilities. In ZSIs, both of the power switches in a leg can be turned on at the same time and thereby eliminate the dead time. This significantly improves the reliability and reduces the output waveform distortion. Fig. 1(a) shows the classical ZSI in which the two-port impedance network couples the main inverter circuit to the dc source. In order to overcome the shortcomings of the classical ZSI, the quasi-ZSI (qZSI) shown in Fig. 1(b) and SL-ZSI shown in Fig. 1(c) were developed in [10]–[12], and [18].

Despite the aforementioned merits, the aforementioned ZSI topologies also show the following drawbacks: 1) capacitors are used in the Z-source network, thus high-voltage or large capacity capacitors should be used, which may result in large volume, cost expensive, and reducing the life span of system; 2) it cannot suppress the inrush current and the resonance introduced by Z-source capacitors and inductors at startup, thus causing the voltage and current surge, which may destroy the devices; 3) it regulates boost factor only by adjusting the shoot-through duty ratio.

To solve the aforesaid drawbacks in aforementioned ZSI, a new ZSI topology is presented with no capacitor and reducing inherent inrush current limitation at startup. It can suppress the resonance thoroughly by removing capacitor and improve the efficiency of power supply. The operation principle and comparison with the classical ZSI and SL-ZSI reveal the merits of the proposed topology, and are also verified in both simulation and experiment.
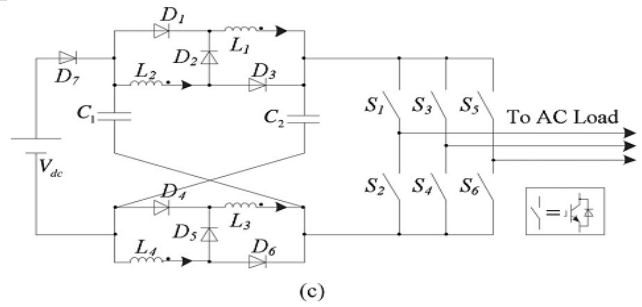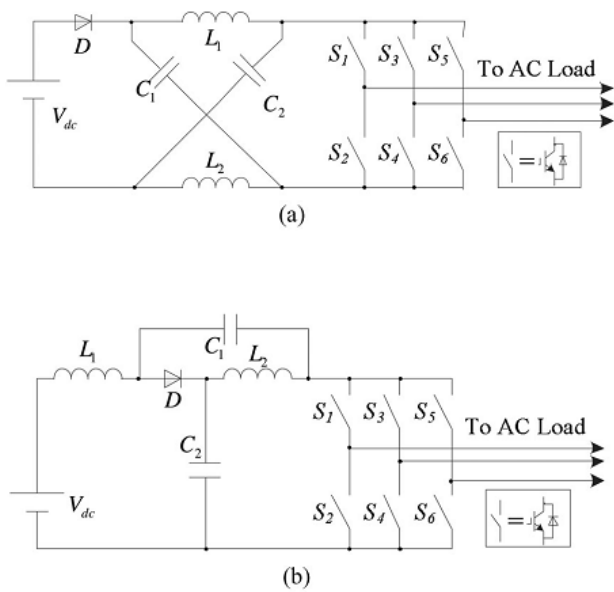

Fig. 1: Conventional impedance-network inverter topologies. (a) The classical ZSI, (b) quasi-ZSI, and (c) SL-ZSI.

II. L-Z-SOURCE INVERTER

Different to the original ZSI, the proposed inverter has no capacitor, and is composed of two inductors (L1 ,L2, and L1 =L2), and three diodes (D1 ,D2, and D3), as shown in Fig. 2. The combination of L2 − L3 − D1 − D2 − D3 acts as a switched-inductor cell. The proposed topology provides inrush current suppression, unlike the traditional topologies, because no current flows to the main circuit at startup. The proposed topology also provides a common ground for the source and inverter.

Unlike the traditional ZSIs, L-ZSI just has shoot-through zero states besides the traditional six active states. The operating principles of the proposed inverter are also similar to those of the classical ZSI. For the purpose of analysis, the operating states are simplified into shoot-through and non-shoot-through states. Fig. 3 shows the equivalent circuits of L-ZSI.

In the non-shoot-through state, as shown in Fig. 2, D2 is on, while D1 and D3 are off. L1 and L2 (L1 = L2 = L) are connected in series. L1 and L2 transfer energy from the dc voltage source to the main circuit, and the equivalent circuit is shown in Fig. 3(a). The corresponding voltages across L1 and L2 in this state are V1_non and V2_non, respectively. Thereby, (1) and (2) can be contained

$$V_{1\_non} + V_{2\_non} + V_i = V_{dc} \qquad (1)$$

$$V_{1\_non} = V_{2\_non} \qquad (2)$$

From (1) and (2), (3) and (4) can be concluded

$$V_{1\_non} = \frac{1}{2}V_{dc} - \frac{1}{2}V_i \qquad (3)$$

$$V_{2\_non} = \frac{1}{2}V_{dc} - \frac{1}{2}V_i \qquad (4)$$
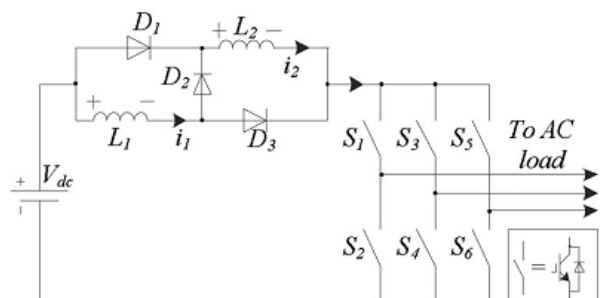
Where Vdc is the dc source and Vi is the dc-link voltage.

(a)

(b)

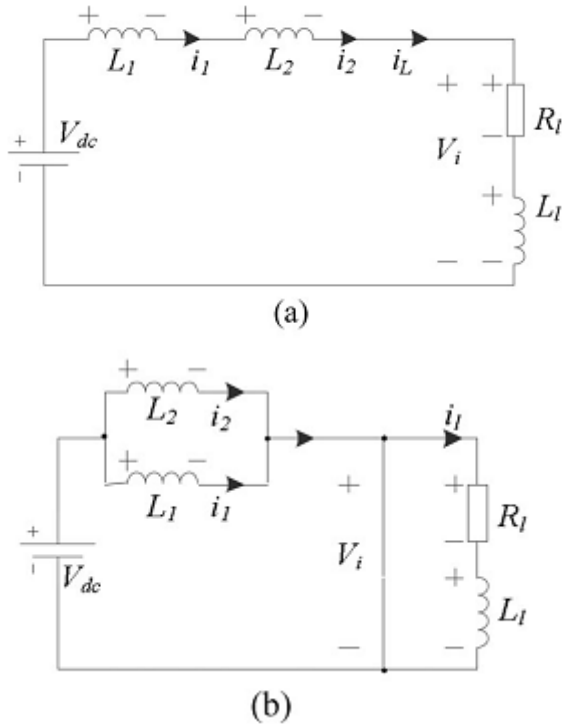Fig 2: L-ZSI with two inductors.

(a)

(b)

Fig. 3: Operating states: (a) non-shoot-through and (b) shoot-through state.

In the shoot-through state, as shown in Fig. 2, the inverter side is shorted by both the upper and lower switching devices of any phase leg. During the shoot-through state, D2 is off, while D1 and D3 are on. L1 and L2 are connected in parallel, and inductors L1 and L2 store energy. The equivalent circuit is shown in Fig. 3(b). The corresponding voltages across L1 and L2 in this state are V1 and V2, respectively, and (5) is obtained

$$V_1 = V_2 = V_{dc} \qquad (5)$$

Applying the volt–second balance principle to L1 and L2, (6), (7), (8), and (9) can be obtained from (3), (4), and (5)

$$V_i = \frac{1+D}{1-D} V_{dc} \qquad (6)$$

$$B = \frac{1+D}{1-D} \qquad (7)$$

$$I_L = I_1 = I_2 = \frac{D(2L + L_l) + L(1-D)}{R_l L(1-D)} V_{dc} \qquad (8)$$

$$I_l = \frac{(1+D)}{R_l} V_{dc} \qquad (9)$$

Where B is the boost factor; IL is the inductor current; Il is the load current; D is shoot-through duty cycle; I1 and I2 are current of L1 and L2, respectively; Rl is load resistance; Ll is load inductance.

When Ll = 0 or load is resistive, (10) is obtained

$$I_L = I_1 = I_2 = \frac{(1+D)}{R_l(1-D)} V_{dc} \qquad (10)$$

III. DIODE CLAMPED MLI

Most attractive features that make multilevel inverters to be applied in various applications are, they can generate output voltages with extremely low distortion, draw input current with very low distortion, generate smaller common-mode voltage thus reducing the stress in the motor bearings, able to operate with lower switching frequency etc. Electrical energy production from batteries gives DC output voltage, so inverters are a compelling solution to convert output voltage of batteries into alternative form especially when AC loads are used. Due to advantages of multilevel inverters over the conventional three level inverters, they are used for renewable energy applications when AC loads are used. A diode clamped multilevel inverter with 5 level voltage generations is shown in Figure 4.

Diode-clamped multilevel Inverters found applications in the areas of static var compensation, variable speed motor drives, and high-voltage system interconnections. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is V_{in}, and the voltage stress across each switching device is limited to V_{in} through the clamping diodes. The principal advantages of a diode clamped multilevel inverter include the following: 1. All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. 2 .The capacitors can be pre-charged as a group. 3. Efficiency is high for fundamental frequency switching.
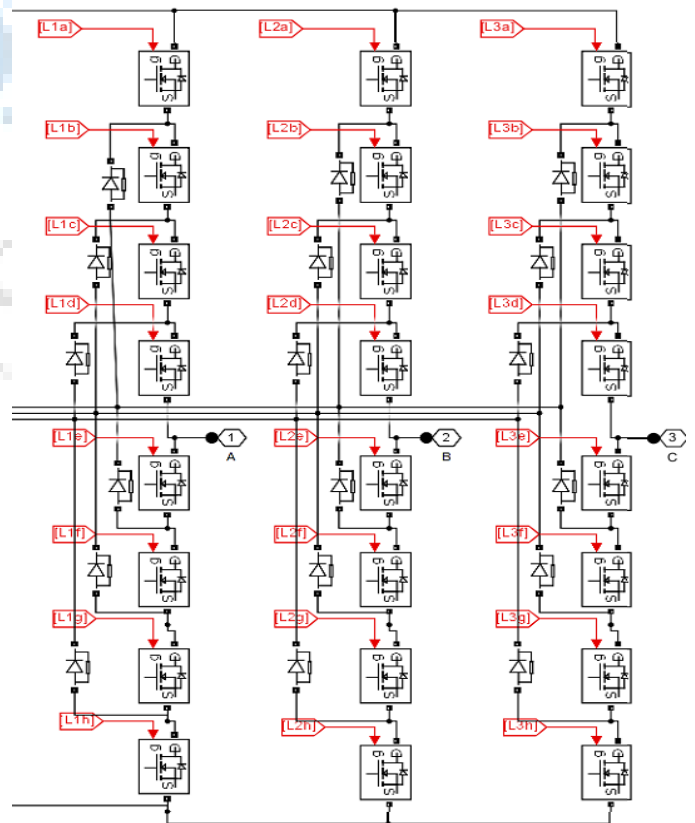

Fig 4: A 3 Phase Diode Clamped MLI for 5 Level volatge generation.

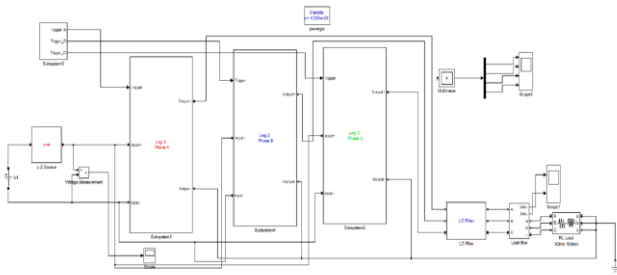### IV. MODEL SIMULATION & RESULTS

Fig 5: Simulation diagram of LZ Source Inverter with 11 Level Diode Clamped MLI

Model schematic of LZ Source based diode clamped multilevel inverter is shown in figure 5. The multilevel inverter is controlled with sinusoidal pulse width modulation. The proposed circuit is simulated for different kinds of load. The voltage available at the output terminals of LZ Source is given in fig 6. Voltage available across the load terminals and current through the load are presented in figure 7 and 8 and total harmonic distortion in the output voltage and current for a load resistance of 100 Ohm and inductance of 1 mH are shown in fig 9 and 10 respectively.
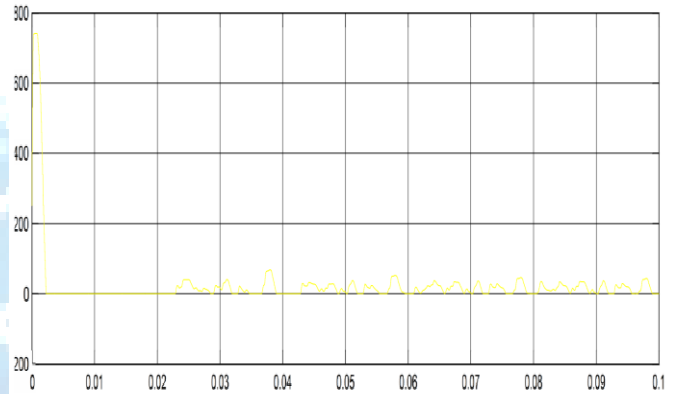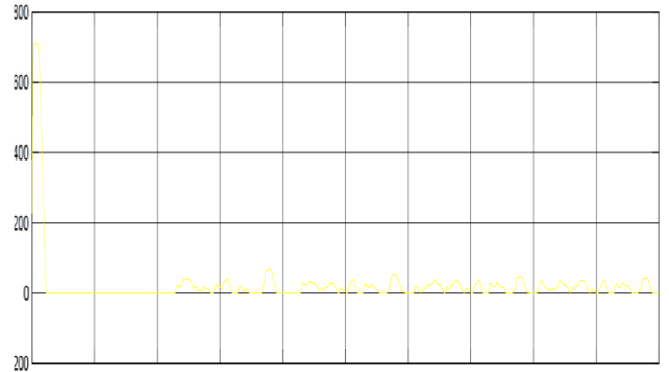

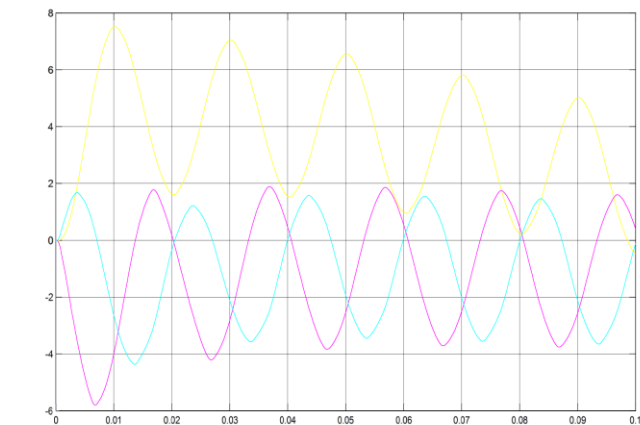**Fig 6:** Current through the inductors of LZ Source Converter
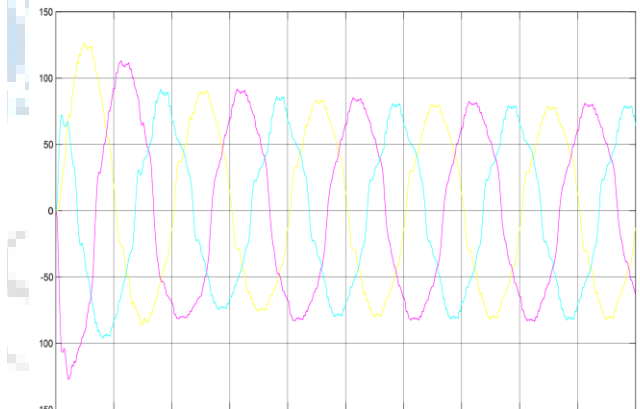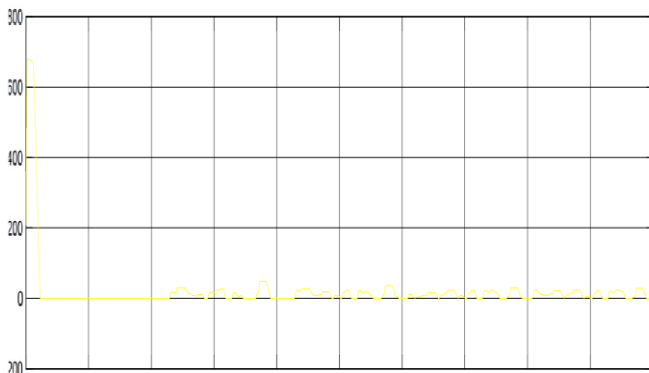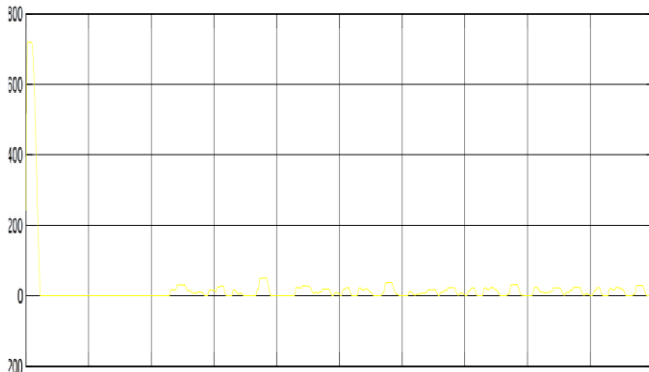

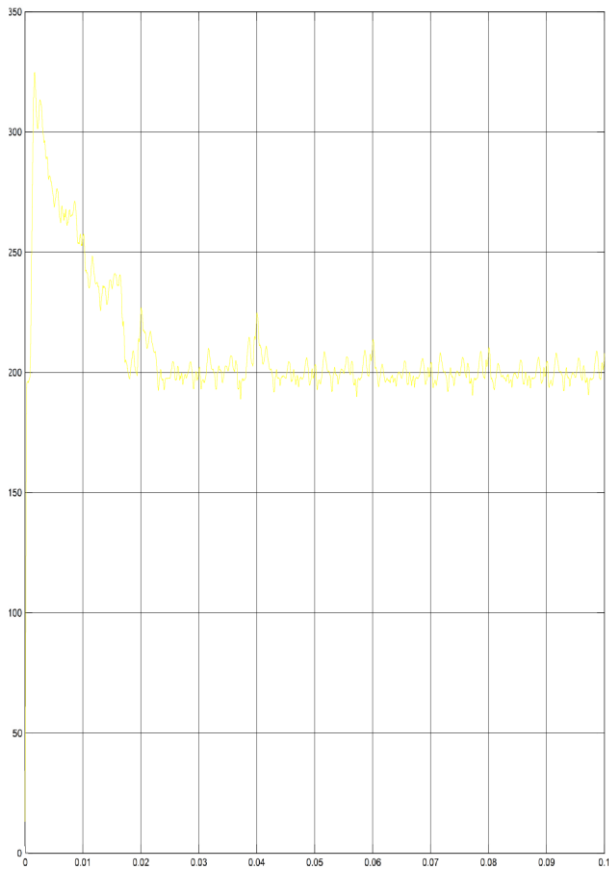**Fig 7:** Voltage across load and Current through load for Load with 0.9 pf lagging.

Fig 8: Voltage across the output terminals of LZ Source.

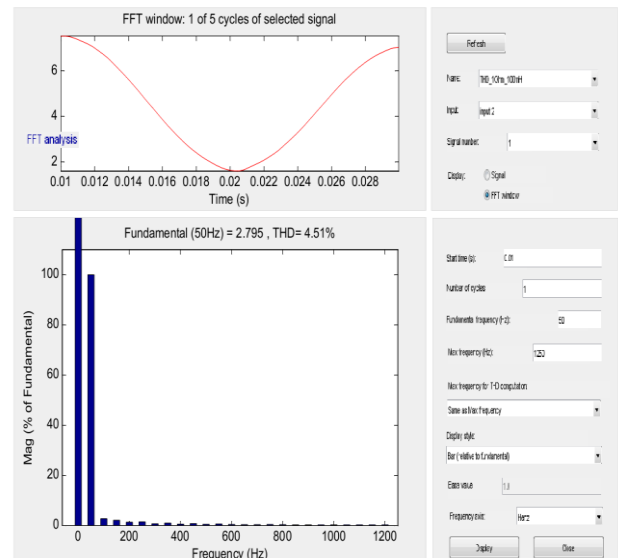**Fig 9:** Total Harmonic Distortion in output voltage.

Fig 10: Total Harmonic Distortion in Load Current.

V. CONCLUSION

Z Source inverters operates as current source inverters. To enhance the current carrying ability of inverters the z source is replaced with LZ source. This LZ Source is coupled to a 11 level diode clamped inverter. It has been observed that the multilevel level inverters will give better quality output in terms of total harmonic distortion, less distorted voltages. In the proposed converter also the same observations are made. In addition to the regular observations the following are achieved by the converter specifically.

1. The converter circuit is used for loads that require high magnitudes of currents for its loads.
2. The switches that are used in LZ Source are subjected to less voltage stress and a uniform dc voltage is available across the output terminals of LZ source.
3. The Voltage available across the output terminals of configuration exhibits less total harmonic distortion, this results in less magnitude of filters.
4. By connecting a filter across the output terminals the distortion in output voltage and current further reduced and give more sinusoidal voltages and currents.

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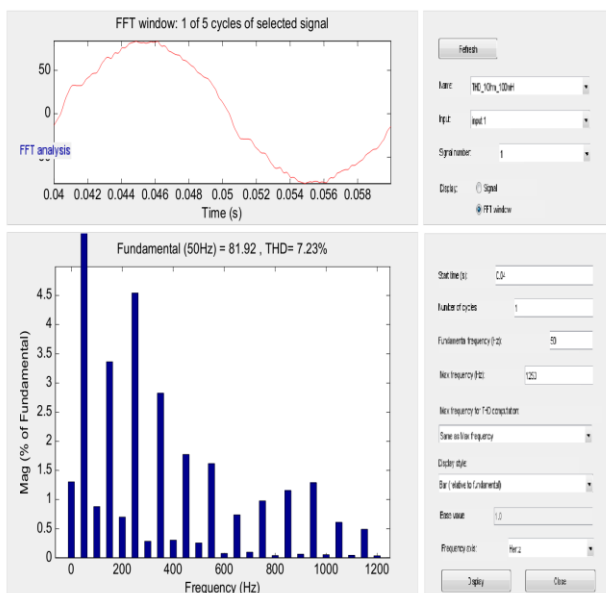[5]. X. Liu, P. C. Loh, P. Wang, and X. Han, "Improved modulation schemes for indirect Z-source matrix converter

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