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RESEARCH ARTICLE

Optimize Design of full subtractor using 45nm Technology

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ABSTRACT

In the recent years low power consumption has become one of the primary requirements in digital vlsi design.With scaling down of device dimensions, for reliable operation, the supply voltage also needs to be scaled down. On reducing the supply voltage for a given technology the speed of conventional digital integrated circuits is degrading. Therefore, there is a need to explore new methodology for the design of digital circuits well suited for high speed and low power consumption. GDI (Gate Diffusion Input)is one of the new digital design technique to achieve high speed, small size and low power consumption. This paper presents the design of full subtractor using full swingi.ehigh noise margin gate diffusioninput (FSGDI) technique whose performance has been compared with full subtractor circuits employing CMOS, transmission gates (TG),) and gate diffusion input (GDI). It has been observed that the FSGDI based full subtractorhas good noise margin compared to GDI technique and less number of transistor count compared to CMOS.

Keywords: GDI, FSGDI, low power,Full subtractor.

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INTRODUCTION

In consumer electronics there are great efforts to achieve low voltage and low power circuit design having utility in portable electronics [1]. The design of digital VLSI circuits has been continuously evolving and being motivated by design criteria such as low power consumption, high speed and small chip area [1–3]. Full Swing Gate Diffusion Input (FSGDI) has been proposed for the design of high speed and low power applications both in analog and digital circuits. In this paper, the design of full subtractor using FSGDI has been presented and its performance has been compared with circuits reported in the literature in terms of parameters such as power, delay, and transistor count [3]. Although, gate diffusion input (GDI)circuits can be implemented with less transistors to reduce power, it suffers from reduced voltage swing at the output as reported in [4]. FSGDI allows the design of full subtractor with fewer transistors and shows significant improvement in performance parameters such as power, area and speed with wider output voltage swing. The workability of proposed full subtractor has been ascertained by CADENCEVIRTUOSO 45nm CMOS technology with supply voltage of 1 V.

2. FULL-SWING GDI

Gate Diffusion Input technique is a new low power technique for digital VLSI design. The basic GDI cell consists of only two transistors and there are three terminals i.e. Gate, Source and Drain are the transistor inputs.

G-common input to gate terminals of pMOS and nMOS. P- input to source or drain terminal of pMOS N- input to source or drain terminal of nMOS VDD and GND are connected to the body of both pMOS and nMOS respectively.

GDI technique also has the advantage of less delay and reduced area. But the disadvantage of GDI is the output does not have a full swing of logic 1 and logic 0. This degraded output is referred to as reduced swing [4]. This paper addresses this issue of reduced swing and provides solution for obtaining a strong 1 and strong 0 at the output of a GDI cell. First an XNOR gate is implemented using basic GDI cell and it is shown how the output has a reduced swing for both logic 1 and logic 0. The XNOR logic gate was employed with additional transistors [3] to obtain the full positive (Strong 1) and negative (Strong 0) swings named as full- swing GDI.

2.1 GDI XNOR gate:

A 1-bit full subtractor basic gate required is xnor gate. The cmos xnor gate requires12transistors but by using GDI only 4 transistors required as shown in fig.1.

As mentioned above, GDI gives weak0 and weak 1 depending on the input a and b. The simulation waveform of 4 Transistor GDI XNOR gate is shown in fig 2. In this waveform, when inputs A and B at logic 1, the XNOR output is weak logic1 and also for A=0, B=1 output is weak logic 0.

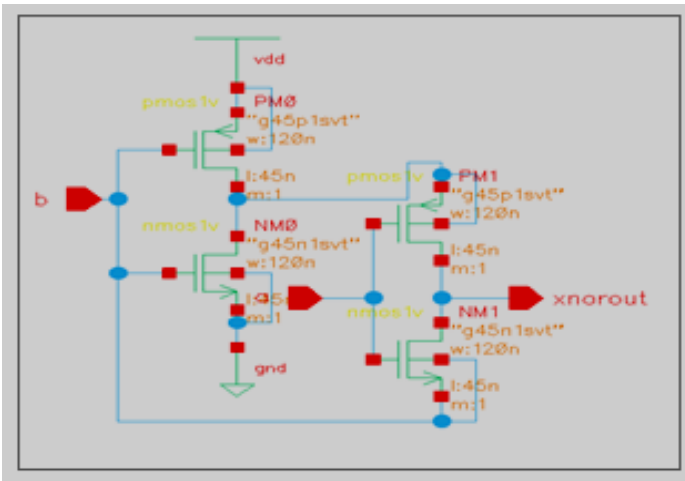


Fig1: GDI XNOR gate

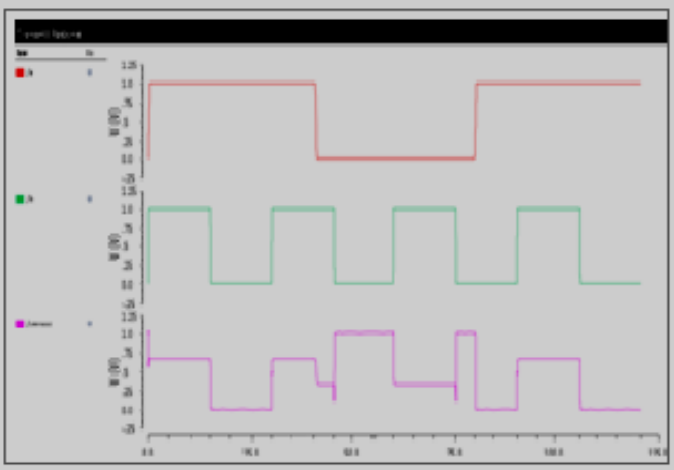


Fig 2: simulation waveform of GDI XNOR gate

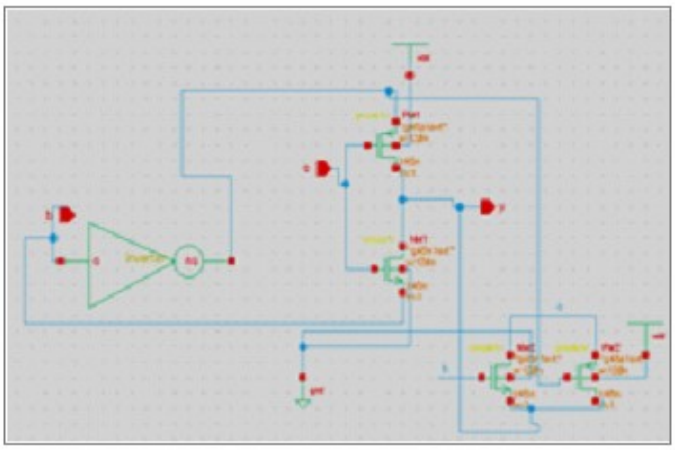


Fig 3: Full Swing GDI XNOR gate

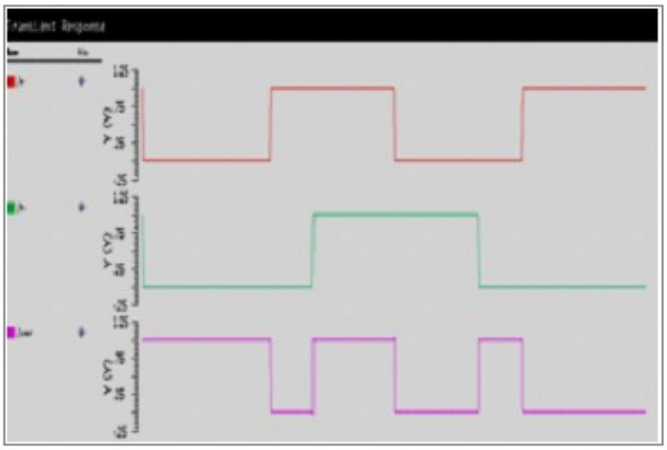


Fig 4: simulation waveform of Full-Swing GDI XNOR gate

In order to improve the output logic swing extra two swing restoring transistors added as shown in fig 3. It requires only 2 extra transistors in order to obtain both strong 0and 1 at the output of the XNOR as depicted in the simulation results (fig 4).

The average power of XNOR gate using 4 and 6 Transistors GDI technique and CMOS technique are calculated from the simulation waveform. The average power results obtained from Cadence Virtuoso for 45 nm technology shown in Table 1.

Table 1: average power of XNOR gate

XNOR	AVGPWR (nw)
GDI(4TR)	52.6
FSGDI(6TR)	16.5
CMOS(12TR)	84.6

3. DESIGN OF FULL SUBTRACTOR

3.1 Conventional full subtractor:

A full subtractor is one of the module used to design ALU of a processor The subtraction of two binary numbers is done by taking the complement of the subtrahend and adding it to the minuend. The full-subtractor is a combinational circuit which is used to perform subtraction of three bits. It has three inputs, A(minuend) and B(subtrahend) and Bin (borrow -in) and two outputs D (difference) and Bout (borrow-out). The Conventional Full Subtractor using gates is as fig. 5. The Truth table is as show in Table 2.

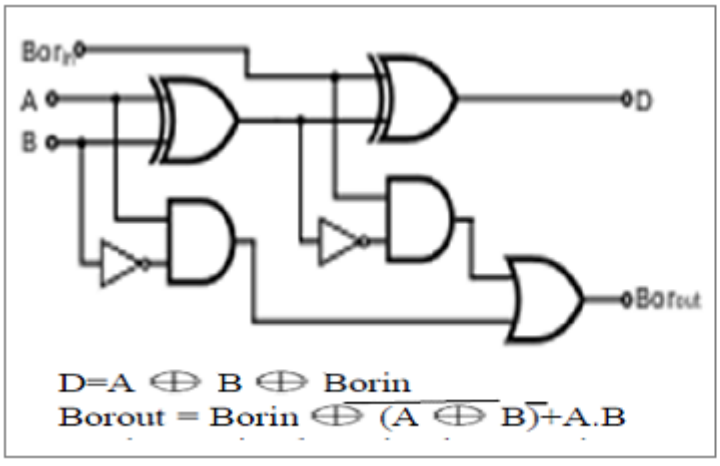


Fig 5: conventional Full subtractor.

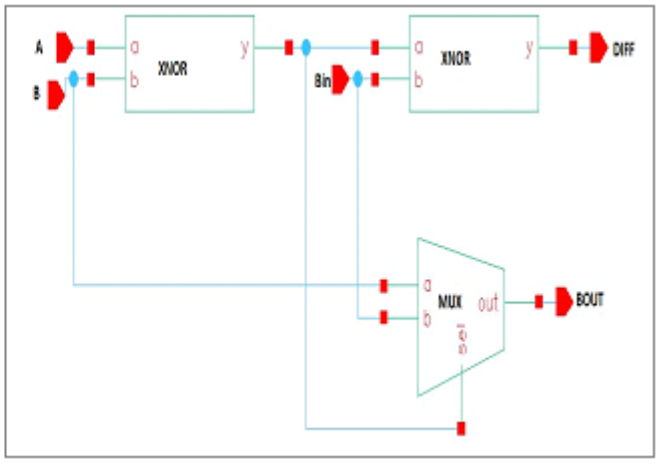


Fig 6: Schematic of Full Swing GDI XNOR based 1-bit full subtractor.

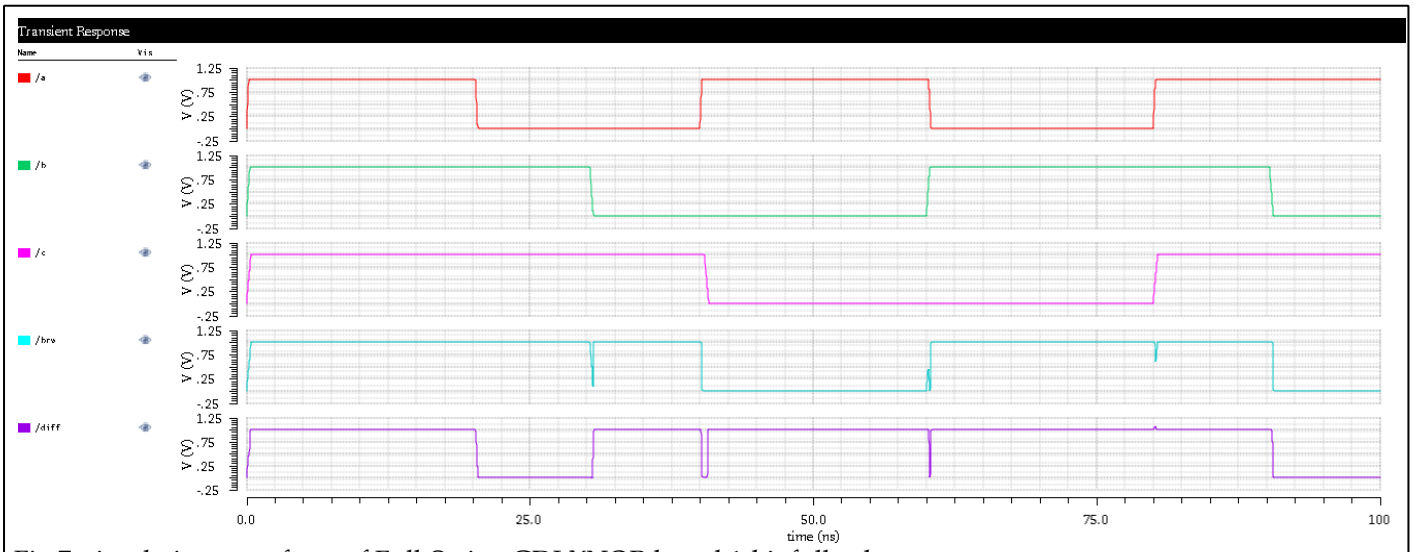


Fig 7: simulation waveform of Full-Swing GDI XNOR based 1-bit full subtractor.

Table 2: Truth table of Full subtractor.

A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

3.2 Proposed Method

The primary goal is to reduce the transistor count to reduce area, power and delay parameters. The proposed full subtractor is designed by XNOR-MUX based full subtractor to reduce the count of transistors and power when compared to conventional CMOS and GDI. The performance a criterion of each module is individually designed from schematic level to layout level is shown in fig 6, 7. and fig 8. shows subtractor simulation. The proposed full subtractor is compared with CMOS logic and shown comparison table. (See Table 3.)

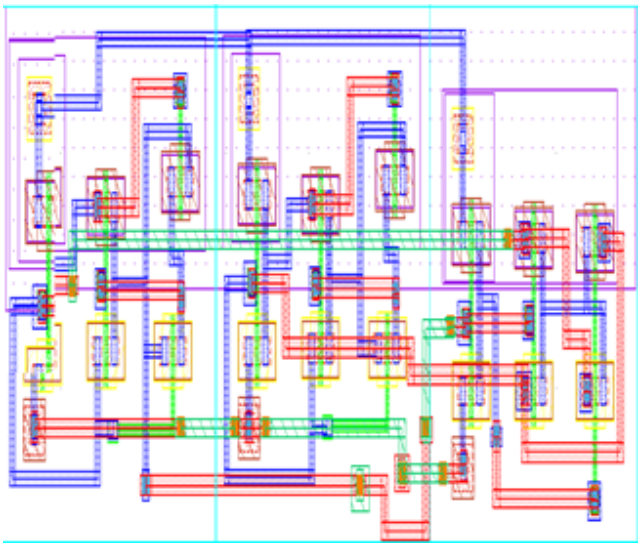
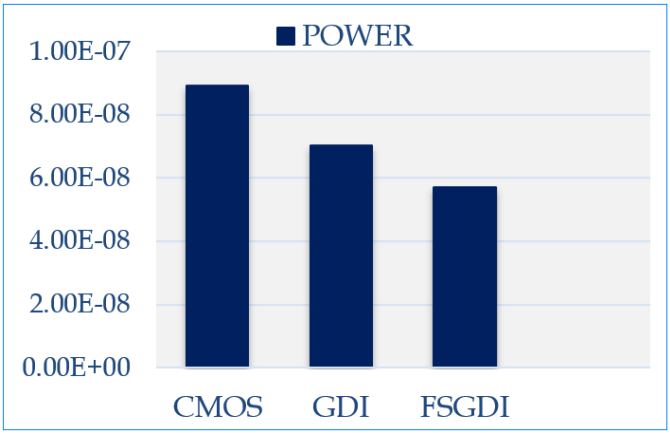


Fig 8: layout of Full-Swing GDI XNOR based 1-bit full subtractor.

Table 3: Simulated results:

parameters	Full- Swing GDI	CMOS	GDI
Power(nw)	57.11	89.23	70.23
Delay(psec)	176	286	195
Transistor count	18	34	10



CONCLUSION

In this paper, Full Subtractor is designed using full-swing GDI and compared its performance with conventional CMOS. The proposed full subtractor reduces the area , delay, and power consumption when compared to CMOS and GDI . Full swing GDI is one of the effective techniques among the PTL (Pass Transistor Logic) and other logic style. The Conventional CMOS Subtractor requires 34 transistors which is reduced to 18 transistors in the proposed circuit. The simulation results reveals better noise margin, power and area compared to CMOS logic design styles.

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