Experimental Analysis of the Variants of UBCT Amplifier Circuit

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Abstract:
The Unipolar-Bipolar Composite Transistor (UBCT) circuit is designed to combine the advantages of high input resistance of unipolar transistor and transfer curve linearity of bipolar transistor. The Composite Circuit has been designed with n-channel JFET, npn BJT and a pair of resistors, therefore this type of JFET-BJT composite transistor is classified as UBCT. This UBCT circuit exhibits enhanced static and dynamic performances as compared to that of JFET. In the present correspondence, the performances of the variants of the UBCT amplifier circuit have been experimentally analysed on the basis of power dissipation level and the corresponding voltage gain of the amplifier. According to the experimental results, the UBCT amplifier circuit can be used as a power efficient small signal amplifier for analog applications.

Keywords— Composite Transistor, CT, Unipolar-Bipolar Composite Transistor, UBCT, JFET-BJT Composite Transistor, M-FET, UBCT Amplifier.
The gate of JFET works as well as the final gate for UBCT. According to this UBCT circuit topology, it can also be fabricated by BIFET MIC technology and designated as a three terminal composite transistor device as depicted in fig.1.

This type of UBCT is specifically considered as a simplified circuit design of earlier reported JFET-BJT composite transistors [8]. The circuit components of UBCT (JFET-BJT composite transistor) have been optimized for parametric enhancement [9]. According to the static performance, it also offers wide range linearity in transfer curve and very high input resistance [10]. The drain resistance and trans conductance curves also exhibit linearity over the wide range of drain-to-source voltage and gate-to-source voltage respectively up to the pinch-off value of UBCT [11]. The dynamic performance of UBCT circuit promotes its application as an efficient small signal amplifier [12].

III. UBCT AMPLIFIER CIRCUIT

This UBCT is used as an active component in a common source amplifier circuit as depicted in fig.2. The circuit is biased under the source self-biasing topology of JFET amplifier with an applied ac source capacitively coupled to the gate input. The output of the amplifier is obtained at the drain end of the UBCT. The source self-biasing or self-biasing is basically a current series feedback circuit in which the source feedback resistor $R_{S1}$ is used to provide Q-point stabilization against change in transistor parameters and variation in temperature.

The feedback voltage is developed across source resistor $R_{S1}$ and the negative feedback can also be invalidated by using the source bypass capacitor $C_{S1}$, which keeps the source of the UBCT effectively at ac ground [13]. The gate resistor $R_G$ can be large, usually of $1\,\text{M}\Omega$, which serves to maintain the average gate voltage at ac ground [14]. Also the large value of $R_G$ prevents loading of the ac signal source. The passive circuit components used in UBCT amplifier e.g. the resistors and capacitors along with the operating supply voltage have been optimized by a sequence of different sets of experimental observations for procurement of possible parametric boosts. The experimental results confirm that passive components have been optimized at their standard values e.g. the load resistor $R_L=1\,\text{k}\Omega$, gate resistor $R_G=1\,\text{M}\Omega$, source resistor $R_{S1}=100\,\text{\Omega}$, input & output coupling capacitors $C_I=C_O=10\,\text{\mu F}$, source bypass capacitor...
versus the supply voltage \( V_{DD} \) in fig. 3. These observations are plotted in the graph shown.

1k \( \Omega \) resistor pair \( R_{S}-R_{E} \), \( 10k\Omega-1k\Omega \), \( 1k\Omega-100\Omega \), \( 100\Omega-100\Omega \) and \( 100\Omega-10\Omega \) with the supply voltage ranging from 9V to 24V DC and input ac voltage of 100mV (peak-to-peak) having constant frequency of 1kHz (sine wave). These observations are plotted in the graph shown in fig. 3.

Fig.3 Voltage gain with negative feedback \( A_{VF} \) versus the supply voltage \( V_{DD} \) for the variants of UBCT Amplifier circuits having five different resistor pairs \( R_{S}-R_{E} \).

Specifications: UBCT (JFET BFW10, BJT CL100, \( R_{S}-R_{E} \)), \( R_{L}=1k\Omega \), \( R_{G}=1M\Omega \), \( R_{S1}=100\Omega \), \( C_{L}=C_{G}=10\mu F \), \( C_{S1}=N/C \) in case of negative feedback, \( T=32-35°C \), input ac voltage \( V_{i}=100 \) mV (p-p) of 1kHz.

Based on the experimental observations, it appears that the variants having resistor pair \( R_{S}-R_{E} \) (100\( \Omega \)-10\( \Omega \)) as well as \( 100\Omega-10\Omega \) should be better choices as the voltage gain \( A_{VF} \) of about 8dB has been achieved even at lower supply voltage \( V_{DD}=15V \). At \( V_{DD}=21V \) & 24V, the variant having resistor pair \( R_{S}-R_{E} \) (10k\( \Omega \)-1k\( \Omega \)) also shows better voltage gain. The UBCT variants having resistor pair \( R_{S}-R_{E} \) (10k\( \Omega \)-1k\( \Omega \)) and \( 1k\Omega-1k\Omega \) do not show considerable voltage gains for the entire experimental range of supply voltage from 9V to 24V. The supply voltage \( V_{DD}=21V \) and above, the voltage gains for all the resistor pair \( R_{S}-R_{E} \) are almost about to be saturated. In these observations, the variant of UBCT amplifier circuit having resistor pair \( R_{S}-R_{E} \) (100\( \Omega \)-10\( \Omega \)) exhibits the best performance as the voltage gain \( A_{VF} \) of 13.39dB is achieved at the supply voltage \( V_{DD}=18V \).

(B) Power Dissipation Analysis for UBCT Amplifier Circuit

The objective of power dissipation analysis is to design a power efficient UBCT amplifier circuit which offers the best possible voltage gain at the optimal power dissipation level. The experimental observations for the analysis of power dissipation of UBCT amplifier are plotted in the column graph as shown in fig. 4. The graph depicts the Voltage gain with negative feedback, Total power dissipation of the circuit, power dissipation across Load resistor, UBCT, JFET and BJT respectively for five variants of UBCT circuits consisting of different pairs of source and emitter resistors \( R_{S}-R_{E} \) having values \( 10k\Omega-1k\Omega \), \( 1k\Omega-1k\Omega \), \( 1k\Omega-100\Omega \), \( 100\Omega-100\Omega \) and \( 100\Omega-10\Omega \) at constant supply voltage \( V_{DD} \) of 18V. The supply voltage of \( V_{DD}=18V \) is optimized because the voltage gains of four out of five variants of UBCT have been almost saturated. The power dissipation observations display that the obtained voltage gains for different resistor pairs \( R_{S}-R_{E} \) (10k\( \Omega \)-1k\( \Omega \)), \( 1k\Omega-1k\Omega \), \( 1k\Omega-100\Omega \), \( 100\Omega-100\Omega \) and \( 100\Omega-10\Omega \) are - 0.63dB, 1.87dB, 5.44dB, 9.54dB and 13.39dB respectively.

In view of this, use of the variants of UBCT having resistor pairs \( R_{S}-R_{E} \) (10k\( \Omega \)-1k\( \Omega \)) and \( 1k\Omega-1k\Omega \) are avoided and not to be considered because of their lower voltage gains. The variant of UBCT having resistor pair \( R_{S}-R_{E} \) (1k\( \Omega \)-100\( \Omega \)) also gives a lower voltage gain of 5.44dB with a large total power dissipation level of 242.28mW.
satisfactory results have been obtained by the use of the variants of UBCT having resistor pairs \((R_S-R_E)\) (100Ω-100Ω) and (100Ω-10Ω) with better voltage gains of 9.54dB and 13.39dB at comparable lower power dissipation levels of about 158.58mW and 203.58mW respectively. Overall, the best result is offered by the variant of UBCT having resistor pair \((R_S-R_E)\) (100Ω-10Ω) as compared to that of (100Ω-100Ω) is due to the optimal power dissipation levels of load resistor, UBCT, JFET and BJT.

![Fig.4 Power Dissipation of the variants of UBCT Amplifier circuits having five different resistor pairs](image)

**V. CONCLUSION**

The present paper represents the experimental analysis regarding the performance of the variants of UBCT amplifier circuit. Observations for these variants have been studied precisely by keeping some parameters constant during the experiment e.g. the supply voltage \(V_{DD}\) is kept constant at 18V, the input ac voltage \(V_i=100mV\) (p-p) of 1kHz, load resistor \(R_L=1kΩ\), source resistor \(R_S1=100Ω\), gate resistor \(R_G=1MΩ\), input & output coupling capacitors \(C_I=C_O=10µF\), source bypass capacitor \(C_{Sl}=N/C\) for providing voltage gain with negative feedback and the range of operating temperature is between 32°C to 35°C. According to the experimental observations, the UBCT amplifier circuit having resistor pair \((R_S-R_E)\) (100Ω-10Ω) has performed the best among all other variants as it could be able to deliver the voltage gain of 13.39dB at total power dissipation level of 203.58mW. At this condition, the power dissipation levels of the UBCT, JFET and BJT are 62.77mW, 31.85 mW and 26.50mW respectively, whereas the power dissipation levels of the load resistor is 127.92mW. Since, all these power dissipation levels are in safe region as per the data sheets of the components used in the circuit, hence the designed UBCT amplifier circuit can be used as a power efficient small signal amplifier for analogue applications.

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