International Journal of Engineering Research and General Science Volume 4, Issue 2, March-April, 2016
ISSN 2091-2730

A Review on Pipelined integer DCT architecture for HEVC

Mr. Rahul R. Bendale, Prof. Vijay L.Agrawal

HVPM COET,Amravati, Maharashtra,India, rahulrbendale@gmail.com, 7758022401.

Abstract — Currently different types of transform techniques are used by different video codecs to achieve data compression during video frame transmission. Among them, Discrete cosine transform (DCT) is supported by most of modern video standards. The integer DCT is an approximation of DCT. It can be implemented exclusively with integer arithmetic. Integer DCT proves to be highly advantageous in cost and speed for hardware implementation. Implementation of an efficient discrete cosine transform with reduced complexity and number of multiplications. Pipelining technique is introduced to reduce the processing time. The full pipeline variable block size transform engine with the efficient hardware utilization is proposed to handle the DCT/IDCT.2D-DCT is computed by combing two 1D-DCT that connected by a transpose buffer.

Keywords— Discrete cosine transform (DCT),HEVC,I-DCT,FPGA,VHDL,Video compression

INTRODUCTION

H.265/High Efficiency Video Coding (HEVC) is the successor codec to H.264,which, like H.264, is jointly developed by the ISO/IEC Moving Picture Experts Group and ITU-T Video Coding Experts Group (VCEG)To maximize compression capability and improve other characteristics such as data loss robustness, while considering the computational resources that were practical for use in products at the time of anticipated deployment of each standard. It is widely used for many applications, including broadcast of high definition (HD) TV signals over satellite, cable, and terrestrial transmission systems, video content acquisition and editing systems, camcorders, security applications, Internet and mobile network video, Blu-ray Discs, and real-time conversational applications such as video chat and video conferencing. However, an increasing diversity of services, the growing popularity of HD video, and the emergence of beyond-HD formats (e.g., 4k×2k or 8k×4k resolution) are creating even stronger needs for coding efficiency. Moreover, the traffic caused by video applications targeting mobile devices and tablet PCs, as well as the transmission needs for video-on-demand services, are imposing severe challenges on today's networks. An increased desire for higher quality and resolutions is also arising in mobile applications. HEVC has been designed to address essentially all existing applications of H.264/MPEG-4 AVC and to particularly focus on two key issues: increased video resolution and increased use of parallel processing architectures.

The 2D-DCT is computationally intensive and as such there is a great demand for high speed, high throughput and short latency computing architectures. Due to the high computation requirements, the 2D-DCT processor design has been concentrated on small non overlapping blocks (typical 8x8). Many 2D-DCT algorithms have been proposed to achieve reduction of computational complexity and thus increase the operational speed and throughput. The various algorithms and architectures for the 2D-DCT can be divided into two categories: The row-column decomposition methods and the non-row-column decomposition methods

Literature SURVEY:

- Gary J. Sullivan [1] introduces H.264/AVC video coding standard. The main goal is to enhance compression, performance. The advantage of this paper is that it explains the standardization process. The disadvantage of this paper is that the desired efficiency of video compression couldn't be achieved to that extent.

- Yunqing Ye and Shuying Cheng [3] Implement 2D-DCT Based on FPGA with Verilog HDL Discrete Cosine Transform is widely used in image compression. This paper describes the FPGA implementation of a two dimensional (8×8) point Discrete Cosine Transform (8×8 point 2D-DCT) processor with Verilog HDL for application of image processing. The row-column decomposition algorithm and pipelining are used to produce the high quality circuit design with the max clock frequency of 318MHz when implemented in a Xilinx VIRTEX-Ⅱ PRO FPGA chip.

- Anas Hatim, S.Belkouch [5] Efficient hardware architecture for direct 2D DCT computation and its FPGA Implementation- In this paper, we propose a low complexity architecture for direct 2D-DCT computation. The architecture will transform the pixels from spatial to spectral domain with the required quality constraints of the compression standards. In our previous works we introduced a new fast 2D DCT with low computations: only 40 additions are used and no multiplications are needed. Based on that algorithm we developed in this work a new architecture to achieve the computations of the 2D DCT directly without using any transposition memory. We defined Sk functions blocks to build the 2D DCT architecture. The Sk

block perform 8 function depending on the control signals of the system. The number of additions/subtractions used is 63, but no multiplication or memory transposition is needed. The architecture is suitable for usage with statistical rules to predict the zero quantized coefficients, which can considerably reduce the number of computation. We implemented the design using an FPGA Cyclone 3. The design can reach up to 244 MHz and uses 1188 logic elements, and it respect the real time video requirements.

PROPOSED WORK :

1D DCT : The N-point DCT and inverse DCT (IDCT) of N-point sequence x(n) is defined as [1]:

$$X(k) = e(k)\sum_{n=0}^{N-1} x(n)\cos\left[\frac{(2n+1)k\pi}{2N}\right] \qquad k = 0,1,\dots\dots\dots,N-1$$

$$x(n) = \frac{2}{N}\sum_{k=0}^{N-1} e(k)X(k)\cos\left[\frac{(2n+1)k\pi}{2N}\right] \qquad n = 0,1,\dots\dots\dots,N-1$$

Where, $e(k) = \begin{cases} \frac{1}{\sqrt{2}} & if\ k = 0 \\ 1 & otherwise \end{cases}$

2D DCT : Mathematical representation of N x N point 2D DCT can be written as

$$X(k,l) = e(k)e(l)\sum_{m=0}^{N-1}\sum_{n=0}^{N-1} x(m,n)cos\left[\frac{(2m+1)k\pi}{2N}\right]cos\left[\frac{(2n+1)k\pi}{2N}\right]$$

Where, $e(k) = e(l) = \begin{cases} \frac{1}{\sqrt{2}} & if\ (k,l) = 0 \\ 1 & otherwise \end{cases}$

x(m,n) is 2D input data and *X(k,l)* is transformed DCT coefficients.

Equation for 2D-DCT can be written as follows:

$$X(k,l) = e(k)e(l)\sum_{m=0}^{N-1} cos\left[\frac{(2m+1)k\pi}{2N}\right]\sum_{n=0}^{N-1} x(m,n)cos\left[\frac{(2n+1)k\pi}{2N}\right]$$

In above equation

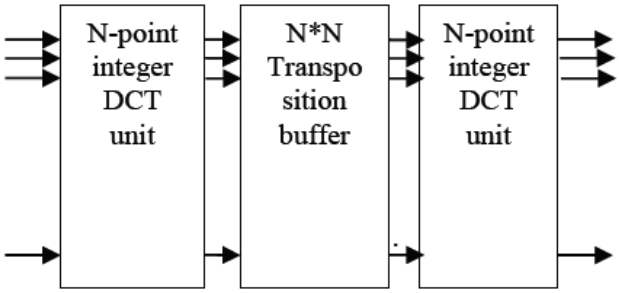
$$\sum_{n=0}^{N-1} x(m,n)cos\left[\frac{(2n+1)k\pi}{2N}\right]$$

represent 1D

DCT of columns of *x(m,n).*

Therefore it is concluded that calculating 1D DCT of columns followed by 1D DCT of rows results in 2D DCT coefficients of 2D input data.Using the separability property of 2-D DCT/IDCT the 2-D transform can be carried out with two passes of 1-D transforms. allows the transform to be applied on one dimension (row) then on the other (column).

Parallel synthesizable implementation of 2D DCT in VHDL. By default it would work on 8 bit input data using 12 bit DCT coefficients (12-bit DCT output). Multiplier-less design, parallel distributed arithmetic with butterfly computation would be used. Implementation would be done as row-column decomposition, two 1D DCT units and transpose matrix between them (double buffered as ping-pong buffer for performance). Following is the probable block diagram for 2D DCT structure using two 1D DCT blocks; one for row and one for column.



To implement VHDL code in Xilinx Self-verifying testbench would be written which would include take matlab-converted image as input.Designed core would transforms it to DCT coefficients and behavioral IDCT testbench code would reconstruct original image from it. PSNR would be computed between original and reconstructed image to find out error introduced by fixed point arithmetic.

In addition Matlab scripts would be written for computing floating point DCT/IDCT as reference for cross checking the DCT values calculated by our designed core. Also, scripts for converting 8 bit bitmap to txt format would be needed so that it becomes readable by testbench and vice versa.

Finally, designed core would be tested on Spartan 6 or Virtex 5 FPGA board as per decided by the memory required for our code.For reconfigurable structures so that it can work with 16, 32 bits etc, we have to just increase the ROM memory sizes and the input data feed line width. But it would take more latency in our parallel pipelined structure as the no. of bits increase.

CONCLUSION

In this paper we have proposed a very low complexity DCT approximation by the row column decomposition for computation of 2D-DCT. Parallel process causes latency in the system. Using the Row-Column decomposition algorithm, the number of calculations are logically reduced. The row column decomposition method reduces the hardware complexity as per the other methods.

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