# PV Fed Non Isolated DC-DC Boost Converter

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**Abstract-** This paper deals with a new topology of the high static gain non-isolated DC-DC boost converter with central point on its output. Proposed converter is a high step up converter. The proposed converter is obtained from the three level boost converter and the quadratic single switch boost converter. The static gain of this proposed converter is bigger than the one from the traditional boost converter and the maximum voltage on two switches is half of the output voltage. Design and hardware implementation of the proposed converter is presented in this paper. The theoretical analysis, design procedure, experimental results and simulation results are presented. The experimental results are compared with simulation results.

**Index Terms**- Photo voltaic (PV), non isolated DC-DC converter, Boost converter, Quadratic single switch boost converter, high step up converter, three level boost converter, Traditional boost converter.

## I. INTRODUCTION

Photovoltaic (PV) power-generation systems are fetching importance and prevalent in distributed generation systems. There are two principal barriers to the use of PV systems: the high installation cost and the low energy conversion efficiency [1]. A conventional centralized photovoltaic array is a serial connection of several panels to obtain higher dc-link voltage for main electricity through a dc–ac inverter [2]. Unfortunately, the power range of a single PV module is usually ranges from 100 Watts to 300 Watts, and the maximum power point (MPP) voltage range starts from 15 V to 40 V. These ratings are low as compared with the essential input voltage for inverters; as it is difficult to obtain high efficiency [3] which will be the input voltage of the inverter; in cases with lower input voltage, it is difficult for the inverter to reach high efficiency [4].

On the other hand, employing a high step-up dc–dc converter in the front of the inverter improves power-conversion efficiency and provides a stable dc link voltage to the inverter. Therefore, in this context, it is necessary to utilize a step-up DC-DC converter as intermediate stage between the Photovoltaic array and the inverter [5].

In addition to the isolated converters with transformers, traditional boost converters can be used for these applications. Within this type of converters, the voltage gain gets reduced because of the losses due to the filter capacitors, inductors, diode rectifiers and the switch operating with high duty ratios. Further, increasing level of the voltage during conversion [6, 7] provides the usage of cascaded boost converter, as the voltage gain of the converters operates with respect to duty cycle. Moreover, the design developed will be bulky and the voltage stress across the main switch will be raised. Applying the similar techniques in [8, 9] the high gain DC-DC converters using coupled inductors are introduced. Using the coupled inductors, with exact winding ratio, voltage stresses across the main switches are suppressed and the reverse recovery of the output diode is more focused. But, the voltage across the output diode remains high and the resonance between the leakage inductance and parasitic capacitor of the output diode cause electromagnetic interference problem and increases losses. Furthermore, the input current ripple is high due to the discontinuity of the current.

A PV panel is a non-linear power source, i.e., its output power/current depends on the terminal operating voltage and the maximum power generated by the system changes with temperature and solar radiation. To increase the ratio of output cost/cost of installation, it is important that PV panel operates at Maximum Power Point (MPP) [10]. Besides, due to the temperature, radiation and load variations, this efficiency can be highly reduced. In order to ensure that the photovoltaic modules always act supplying the maximum power as possible, a Maximum Power Point Tracking (MPPT) controller is employed. In most common applications, the MPPT is achieved through a DC-DC converter controlled through a suitable control strategy.

Basically, a MPPT system consists of a DC-DC converter controlled by a tracking algorithm and the combination of both, hardware and software, defines the tracking efficiency [11]. This work deals with the design and development of a MPP-tracker for photovoltaic systems, which is a high efficiency boost converter operating in continuous conduction mode. The converter is able to draw maximum power from the photovoltaic panel for a given solar radiation level and environment temperature by adjusting the duty cycle of the converter [12].

High gain non-isolated DC-DC boost converter acquired from single switch quadratic boost converter and the three level boost converter presented [13].

## II. PROPOSED CONVERTER TOPOLOGY

The proposed scheme uses a DC-DC converter which is derived from the single switch quadratic boost converter and the three level boost converters. The static gain of the converter depends upon the operating duty cycle and the maximum voltage across the two switches will be half of the output voltage, so that stress across the switches can be reduced.
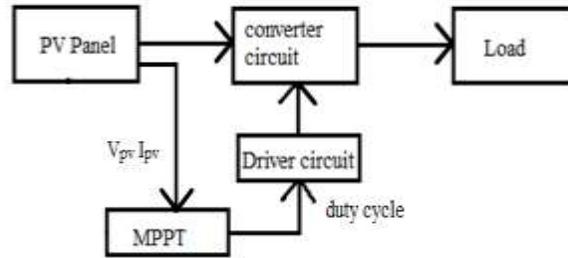
A. Power conversion scheme



Fig. 1. Block diagram of the proposed converter.

The block diagram of the proposed converter connected with the pv panel is as shown in the Fig. 1. The duty cycle for the converter is set based on the photovoltaic voltage and current. The voltage and current of the photovoltaic panel are sensed and is given to the MPPT controller to generate the pulses. To increase the power level of the pulse, driver circuit is used. The driver circuit pulses are given to the boost converter connected with the load.
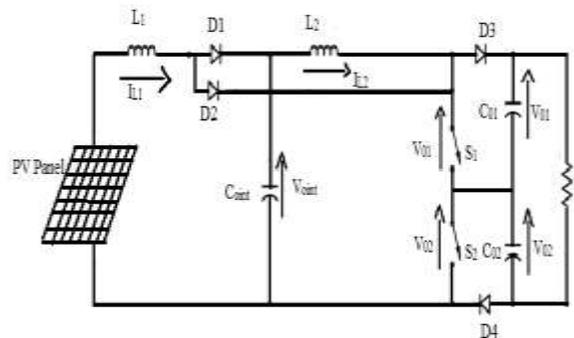


Fig. 2. Proposed high gain DC-DC boost converter.

### III. OPERATION MODES OF CONVERTER

Topology of the proposed converter connected with PV panel shown in Fig. 2. This converter has quadratic static gain as a function of duty cycle. The modulation strategy adopted for the proposed converter is a phase shift PWM modulation. This strategy of modulation results in two pulses of command delayed by 180°. To explain the principle of operation and analyze theoretically the proposed topology, the continuity of the current in both inductors is considered. The Continuous Conduction Mode (CCM) operation in both inductors will be presented. The converter is investigated for regions defined by the values of the duty cycle D (D > 0.5). Different modes of operation of proposed converter are shown in Fig. 3.

The four operation stages of the converter in CCM for duty cycle are greater than 50% (D > 0.5) are presented below. The topological states and the main waveforms of the operation stages are illustrated in Fig. 4.
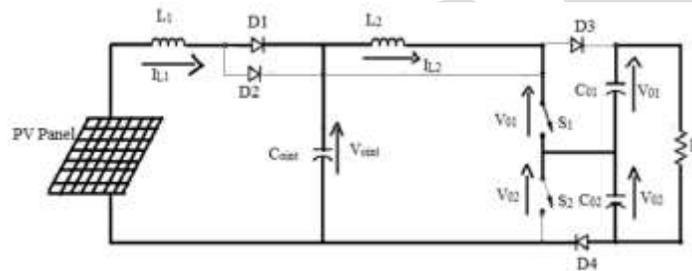
- Mode I $(t_0 - t_1)$

Switches $S_1$ and $S_2$ will be in conduction at the same time, starting the buildup of energy in the inductors $L_1$ and $L_2$. The energy is delivered to load through capacitors $C_{o1}$ and $C_{o2}$, as shown in Fig. 4.
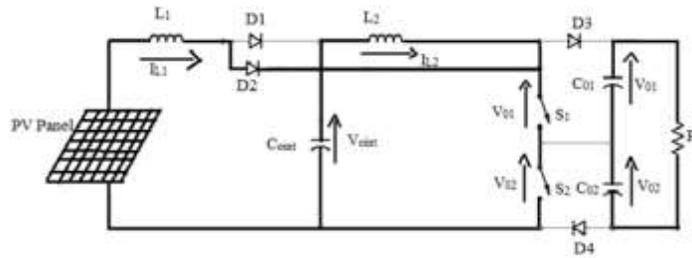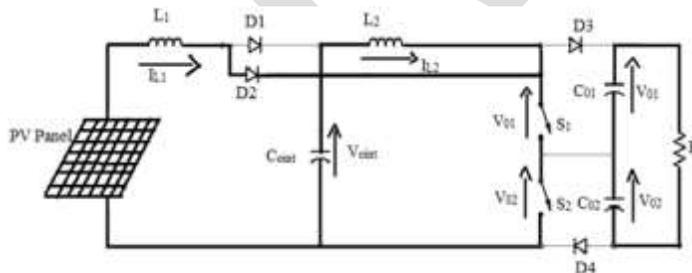
(a)

- Mode II ($t_1$- $t_2$)

Mode II starts when $S_2$ is turned off. The energy is being transferred from input power source to the load. The voltage across $S_2$ is equal to $V_o/2$.
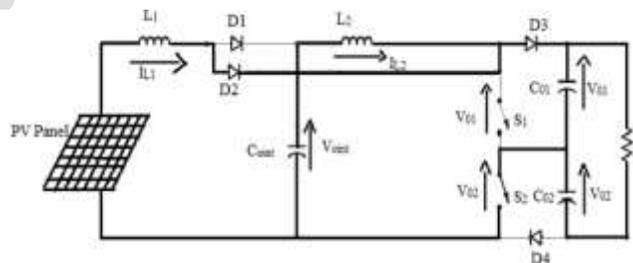


(b)

- Mode III ($t_2 - t_3$)

In mode III the $S_2$ is commanded to turn on again. The topological state and the principle of operation of this stage are equal to the first stage of operation.



(c)

- Mode IV ($t_3 - t_4$)

This stage starts when $S_1$ is turned off and the energy is being delivered to the load. The voltage across $S_1$ is equal to $V_o/2$.



(d)

Fig. 3. Operation modes of converter. (a) Operation of the circuit in mode I.  (b) Operation of the circuit in mode II. (c) Operation of the circuit in mode III.  (d) Operation of the circuit in mode IV.
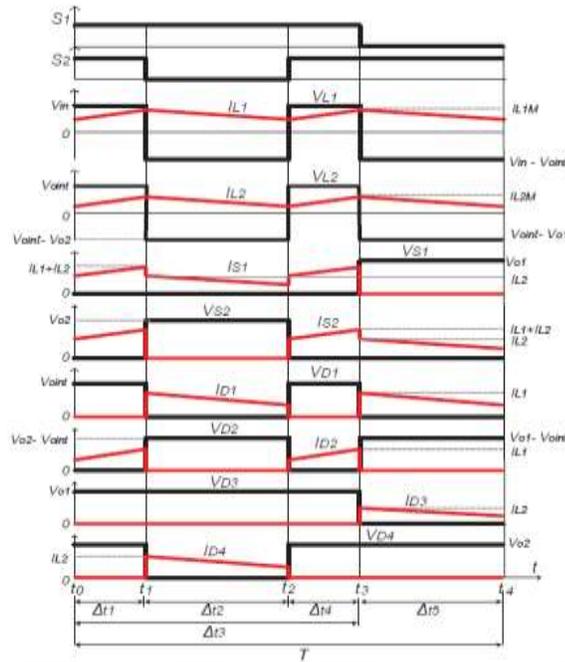


Fig. 4.Theoretical waveforms of the operating stages in CCM for D > 0.5.

## IV. THEORETICAL ANALYSIS OF CONVERTER

According to the main waveforms illustrated in Fig. 4., the relationship between time intervals of each stage of operation as a function of the duty cycle can be defined in (1) and (2).

$$\Delta t_1 = \Delta t_4 = \frac{T.(2.D-1)}{2} \qquad \ldots (1)$$

$$\Delta t_2 = \Delta t_5 = T.(1-D) \qquad \ldots (2)$$

For analysing the steady state characteristics of the proposed high gain DC - DC converter in CCM, some assumptions are to be considered that all the power devices are ideal and capacitors are choosen at higher values to make sure constant output voltage without high ripple content.

The static gain of the converter in CCM for duty ratio D > 0.5 can be evaluated by studying each  conversion stage alone. The partial static gains for the first and second stages of the converter are given by equation (3) and (4). Multiplying (3) and (4) , it is possible to obtain gain is given in equation (5)

$$\frac{V_{oint}}{v_{in}} = \frac{1}{2(1-D)} \qquad \ldots (3)$$

$$\frac{V_o}{V_{oint}} = \frac{1}{(1-D)} \qquad \ldots (4)$$

$$G_{CCM(D>0.5)} = \frac{1}{2.(1-D)^2} \qquad \ldots (5)$$

For the given values of the switching frequency (f), duty cycle (D) and current ripple ($\Delta I_L$), the inductance $L_1$ and $L_2$ are calculated as given in (6) and (7).

$$L_{1(D>0.5)} = \frac{V_0[(1-D)^2(2D-1)]}{\Delta I_{L1}.f} \qquad \ldots (6)$$

$$L_{2(D>0.5)} = \frac{V_0[(1-D)(2.D-1)]}{2.\Delta I_{L2}.f} \qquad \ldots (7)$$

The normalized current ripple ($\Delta I_L$) of $L_1$ and $L_2$ for  region of operations is represented by (8) and (9)

$$\Delta I_{L1} . \frac{L_1 . f}{R_0} = 2 . (1 - D)^4 . (2D - 1) \qquad \dots (8)$$

$$\Delta I_{L2} . \frac{L_2 . f}{R_0} = \frac{(1 - D)(2.D - 1)}{2} \qquad \dots (9)$$

The capacitors $C_{oint}$, $C_{01}$ and $C_{02}$ can be evaluated with a determined voltage ripple ($\Delta V_C$), as given in (10) and (11)

$$\Delta V_{coint} = \frac{2 . I_0 (V_{oint} - V_{in})}{C_{oint} . f . V_{in}} \qquad \dots (10)$$

$$\Delta V_{c01} = \Delta V_{c02} = \frac{2 . I_0 . (2 . V_{c01} - V_{oint})}{2 . C_{01} . f . V_{c01}} \qquad \dots (11)$$

TABLE I : PARAMETERS OF PROPOSED CONVERTER

| Parameters | Values |
|---|---|
| Input voltage $V_{in}$ | 60 V |
| Output voltage $V_{out}$ | 220 V |
| Output power $P_0$ | 220 W |
| Switching frequency | 20 kHz |
| Duty ratio | 61.3% |
| Gain | 3.6 |
| Inductance $L_1$ | 1.15 mH |
| Inductance $L_2$ | 1.812 mH |
| Capacitance $C_{01}$, $C_{02}$ | 100 uF |
| Internal capacitance $C_{oint}$ | 100 uF |

TABLE II : PV PANEL RATINGS

| Parameter | Values |
|---|---|
| $P_{mpp}$ | 250W |
| $V_{oc}$ | 37.25V |
| $I_{sc}$ | 4.35A |
| $V_{mpp}$ | 29.9V |
| $I_{mpp}$ | 8.4A |
| Efficiency | 15.53% |

V.SIMULATION RESULTS OF PROPOSED CONVERTER

The simulation results of proposed converter are obtained for an input of 60V and the output of 220V, at 61.3 percent duty cycle with power rating of 220W at switching frequency of 20 KHz. Parameters of the proposed converter is mentioned in TABLE I. Simulation model of proposed converter is shown in Fig. 5.
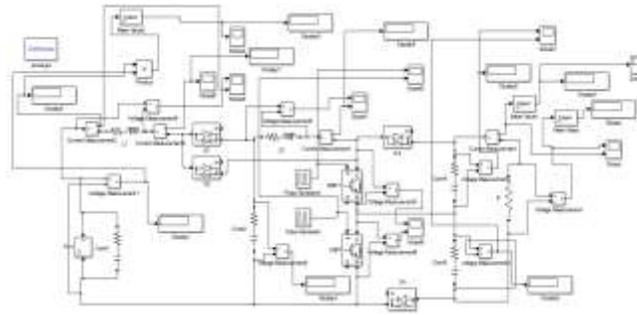
Fig. 5. Simulink model of the proposed converter.

A. Simulink model of the PV panel

Modelling of photovoltaic module is necessary for the design and simulation of photovoltaic system applications because it has non-linear characteristics. Modeling of the solar array (module) is done mainly for obtaining the performance characteristics. The performance characteristics of PV module mainly depend on the operating conditions, they also depend on solar array design quality. The output quantities (voltage, power and current) vary as a function of load current, irradiation, and temperature. The effects of these three variations are considered in the modeling, so that any change in the solar irradiation and temperature levels should not adversely affect the photovoltaic module output. The Simulink model of the photovoltaic module is as shown in the Fig. 6. Photovoltaic module is designed with the ratings as shown in the TABLE II.
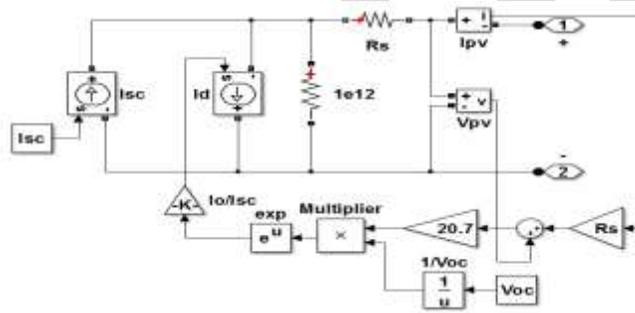


Fig. 6. Simulink of the PV panel.

B.Steady state response for various irradiation levels

Stability of a converter is an essential requirement for any irradiation. Hence, the proposed converter connected with PV panel is tested with different irradiation levels. Simulation results for different irradiation levels are tabulated in TABLE III. Simulation results are shown in Fig. 7.

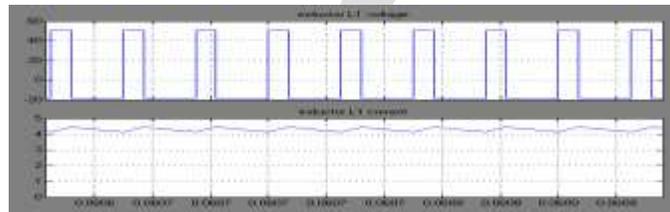TABLE III : SIMULATION RESULTS FOR IRRADIATION LEVELS

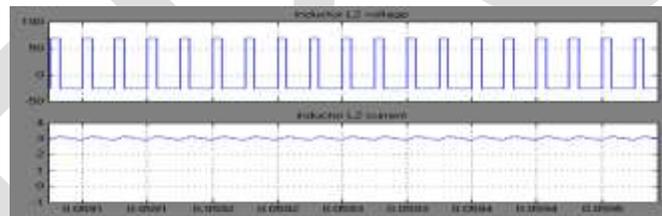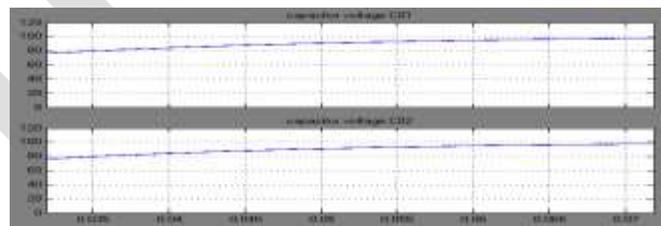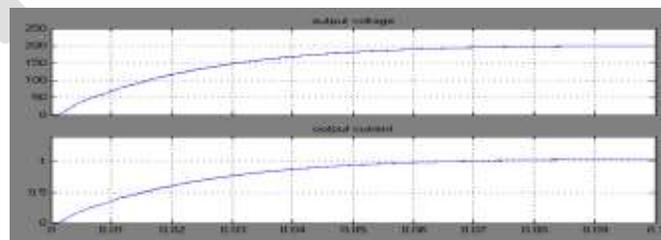| $Q$ | $D$ | $V_m$ | $I_m$ | $P_m$ | $V_0$ | $I_0$ | $P_0$ | $\eta$ |
|-----|-----|-------|-------|-------|-------|-------|-------|--------|
| 0.9 | 62.5 | 57.86 | 3.646 | 218.7 | 190.2 | 0.9804 | 186.47 | 85.3 |
| 0.8 | 61.3 | 56.84 | 3.225 | 190 | 177.2 | 0.9136 | 161.88 | 85.2 |
| 0.7 | 60 | 56.08 | 2.791 | 162.1 | 163.7 | 0.8439 | 138.14 | 85.2 |
| 0.6 | 58.7 | 54.37 | 2.4 | 135.2 | 148.8 | 0.7668 | 114.09 | 85.2 |
| 0.5 | 56.8 | 53.48 | 1.974 | 108 | 133 | 0.6858 | 91.211 | 84.3 |
| 0.4 | 53.42 | 53.42 | 1.517 | 81.6 | 115.5 | 0.596 | 68.838 | 84.4 |
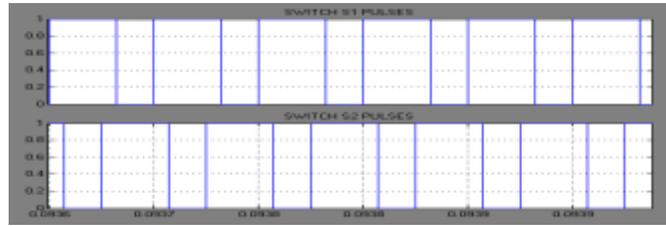
(a)
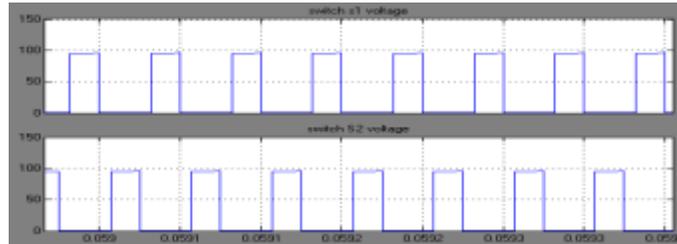


(b)



(c)



(d)



(e)



(f)

Fig. 7. Simulation results of proposed converter. (a) Gate pulses for switch $S_1$ and $S_2$. (b) Voltage across the switches $S_1$ and $S_2$. (c) Voltage and current in inductor $L_1$. (d) Voltage and current in inductor $L_2$. (e) Voltages across capacitors $C_{01}$ and $C_{02}$. (f) Output voltages and output current.

## VI.EXPERIMENTAL RESULTS OF PROPOSED CONVERTER

The experimental results of proposed converter are obtained for the input of 53.8V and the output of 168V, with 220W power at switching frequency of 20 KHz. Hardware model of modified SEPIC converter is shown if Fig. 8.

The values of the inductors and capacitors are calculated using the expressions (4), (5), (6) and (7) considering D = 61%, $\Delta I_{L1(max)} = \Delta I_{L2(max)} = 36$ % and $\Delta V_{oint} = \Delta V_o = 10$ %.
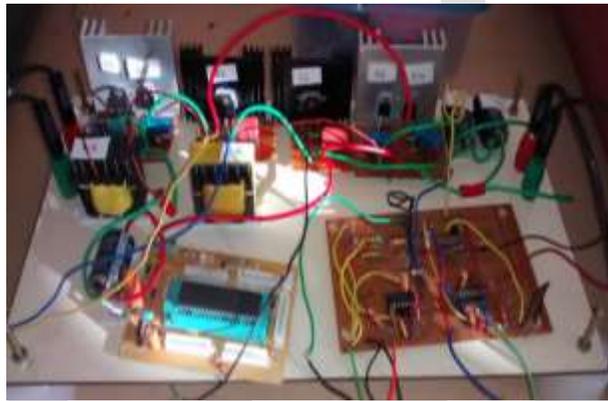


Fig. 8. Hardware model of the proposed converter.

A. Steady state response for various irradiation levels

The proposed converter connected with PV panel with various irradiation levels. Based on the irradiation levels, the duty cycle for the operation of the switches has been set automatically by the microcontroller for obtaining the maximum output power in simulation based on this set values. The results are tabulated in TABLE IV. Experimental results are shown in Fig. 9.

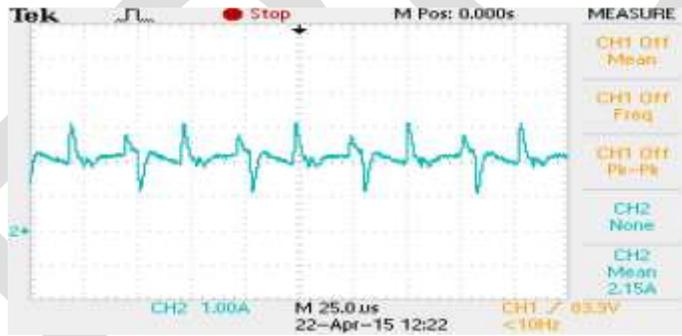### TABLE IV: EXPERIMENTAL RESULTS OF IRRADIATION LEVELS

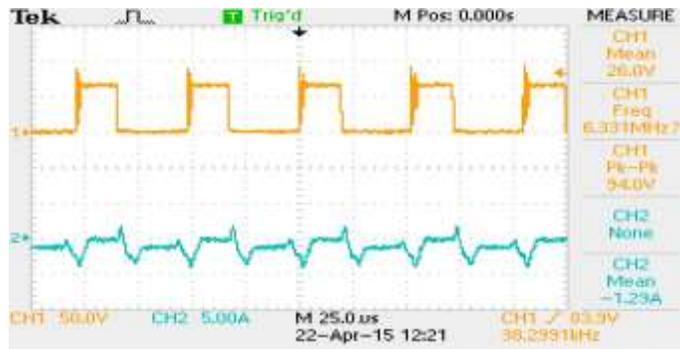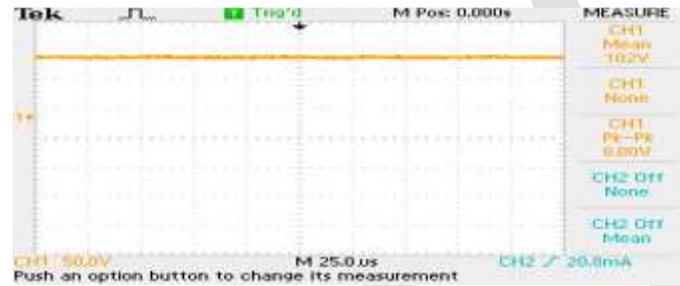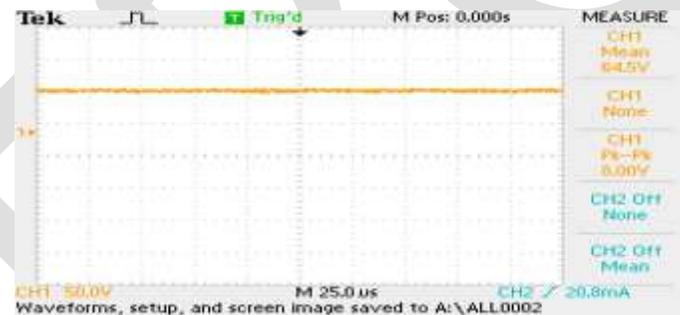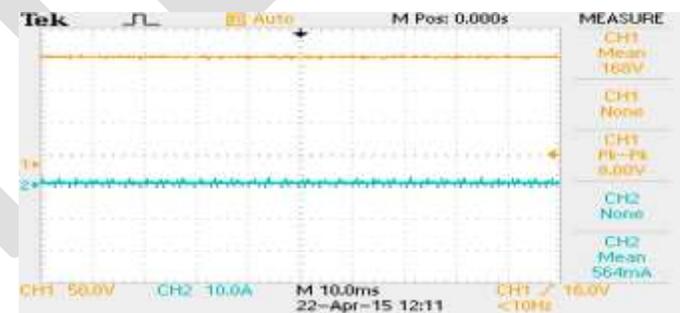| $Q$ | $D$ | $V_m$ | $I_m$ | $P_m$ | $V_0$ | $I_0$ | $P_0$ | $\eta$ |
|------|-------|-------|------|--------|-------|-------|--------|--------|
| 0.9 | 62.5 | 57.8 | 3.64 | 208.08 | 188.7 | 0.924 | 174.35 | 83.78 |
| 0.8 | 61.3 | 56.83 | 3.09 | 166.64 | 166.6 | 0.887 | 147.7 | 88.6 |
| 0.7 | 60 | 56 | 2.67 | 149.52 | 155.3 | 0.825 | 128.12 | 85.68 |
| 0.6 | 58.7 | 54.3 | 2.39 | 129.77 | 137.5 | 0.808 | 111.1 | 85.61 |
| 0.5 | 56.8 | 53.5 | 1.99 | 106.46 | 125.6 | 0.737 | 92.56 | 86.95 |
| 0.4 | 53.42 | 53.5 | 1.53 | 81.6 | 117.5 | 0.612 | 71.391 | 87.85 |
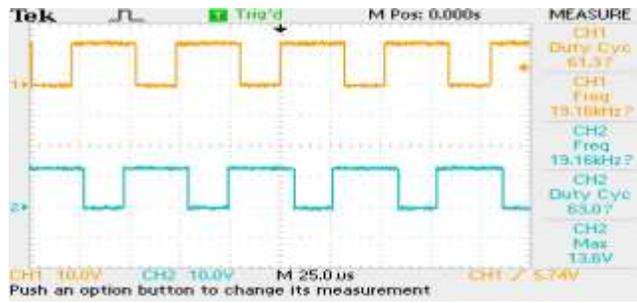
(a)
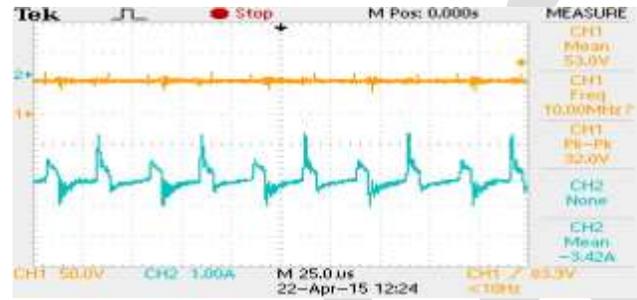


(b)



(c)
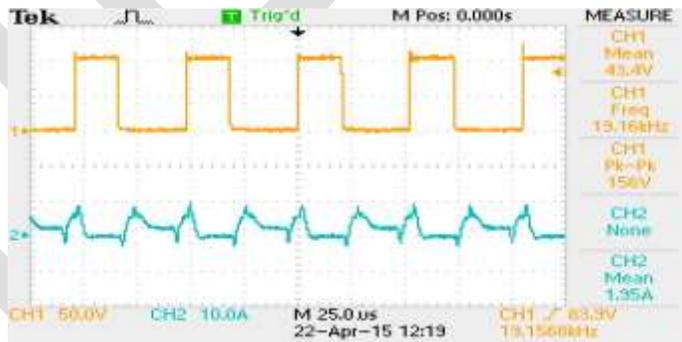


(d)

(e)



(f)



(g)



(h)

Fig. 9. Experimental results of proposed converter. (a) Gate pulses for switches $S_1$ and $S_2$. (b) Input voltage and current through inductor $L_1$. (c) Current through inductor $L_2$. (d) Voltage across and current through switch $S_1$. (e) Voltage and current of switch $S_2$. (f) Voltage across capacitor $C_{01}$. (g) Voltage across capacitor $C_{02}$. (h) Output voltage and current.

## VII. COMPARISON OF SIMULATION AND HARDWARE

A graph is plotted in order to compare the performance of experimental results with simulation results. The graph is plotted by considering the duty cycle Vs power for both experimental and simulation results. The plotted graph is as shown in Fig. 10.
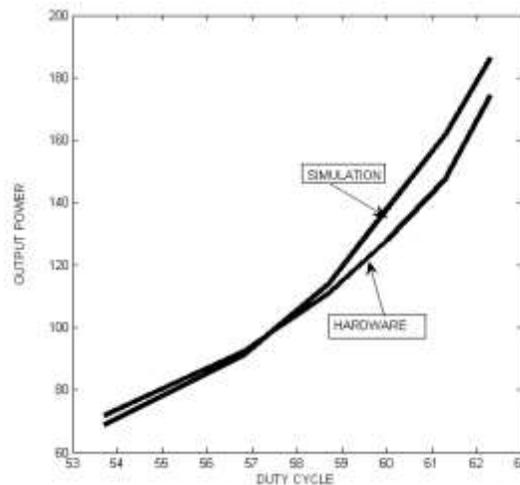


Fig. 10. Comparison of simulation and experimental results.

## VIII.CONCLUSION

From the results, it is clear that proposed converter has higher circuit complexity than a conventional boost converter. The main advantage of the proposed converter circuit it has high gain a given duty cycle. The experimental results and simulation results validates our study.

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