# Time to Amplitude Converter for Phase Shift Detection

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**Abstract**—Time measurement has significant importance in modern science and in its various fields of applications like low and high energy nuclear physics, solid state applications, high energy particle and neutron physics etc. The objective of this paper is to design and develop a Time to Amplitude Converter (TAC) for detecting the Phase Shifts that occur due to time delays, generally in the range of microseconds. Phase Shift can happen due to various complex loads. Therefore, Phase Shifts needs to be measured with high resolution. Phase Shifts are measured in degree or time units. This paper describes the design considerations to be taken into account for selection of components such as integrator, comparator, and ADC that constitutes a TAC circuitry to achieve the desired high speed resolution.

**Keywords**—Time to Amplitude Converter, Phase Shift, Zero Crossing Detector, Propagation Delay, Integrator, Aperture Delay, ADC, Aperture Jitter

## INTRODUCTION

Phase Shift is the difference between two signal waves having the same frequency and referenced to the same point in time. Phase Shift is introduced by complex loads like inductive load or capacitive load or both. [15] Due to Phase Shift, the output signal comes delayed at exit end. In electrical circuit, Phase Shift causes apparent power to increase over the real power making the load to draw more power and thus increases losses. So compensation has to be done to remove the problems caused by Phase Shift.

Of the many techniques, those have been developed for time measurement, conventional method is to measure the time digitally using a counter with a known frequency. But the usage of high frequency crystals can cause noise which disturbs analog circuits. One of the most widely used method in nuclear instrumentation is based on Time to Amplitude conversion (TAC), in which, single channel or multichannel time analysis is used to measure through events that are automatically classified in a built-in time-sorter. A TAC converts the measurement time interval first to a corresponding analogue voltage, which can then be digitized with an analogue-to-digital converter (ADC). [12]

Here, the Phase Shift measurement circuitry has been divided into two parts:
1. Conversion of Time difference to corresponding Analog voltage
2. Analog voltage is converted to Digital by using ADC

The first section comprises of comparators and Integrator which converts the phase shift into corresponding Analog voltage. The second section comprises of ADC unit where signals need to be processed so that the information that they contain can be analysed and displayed

## TAC STRUCTURE & DESIGN

The operating principle of Time to Amplitude Converter (TAC) is as follows: a conversion capacitor is charged by a constant current starting from the rising edge of a START signal until the rising edge of a subsequent STOP signal. This way the voltage across the capacitor increases linearly with time and is proportional to the time interval between start and stop signals. The Time-to-Amplitude Converter (TAC) produces an output pulse with amplitude proportional to the Phase Shift between input "START" and "STOP" pulses. [7]
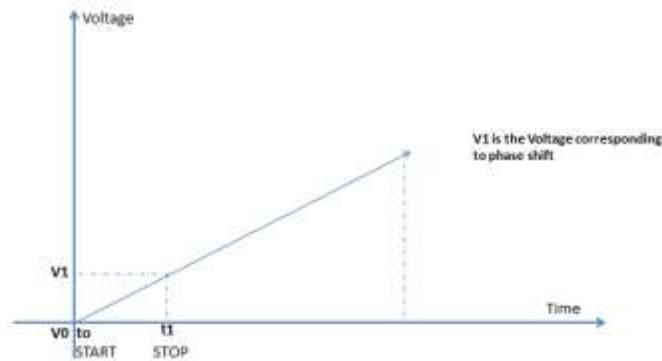
Fig 1.Working Principle of TAC

## 1.1 Block Diagram

The whole structure of the designed TAC is reported in Fig.1. Each module for Phase Shift measurement consists of two channels. Each channel consists of zero crossing detector (ZCD) and Analog to Digital converter (ADC).The integrator which acts as a time reference is common to all channels. The first channel is taken as reference. The input to each ZCD is a sine wave with Phase Shift arriving the channel at time $t_0$, $t_1$ respectively. The output of zero crossing detector in first channel initiates integrator to start a ramp which acts as a START input of TAC and terminate the ramp at a time as per the requirement of user who decides the maximum Phase Shift to be measured. The output of integrator is given as input to all ADCs. The start of conversion for ADCs which acts as a STOP signal of TAC is generated by ZCDs in respective channels. The ADC output is further given to micro controller for processing and output code which represents the Phase Shift is finally displayed on personal computer (PC).
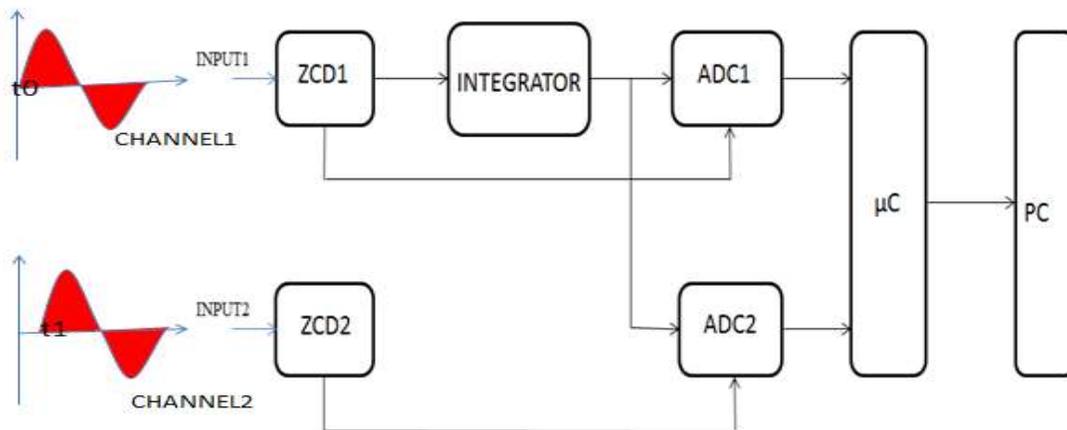


Fig 1.Structure of TAC

## 1.1.1 Integrator

The integrator acts as a time reference and is common to all channels. The integrator generates a ramp whenever a zero crossover is detected from the reference channel. Selecting the proper OPAMP for this application appears to be very important to avoid nonlinearity of ramp for better performance of the system. The important parameters we have to take into consideration are:

*(1)* ***Slew rate*** - This represents the maximum rate of change of an OPAMP's output voltage with time. The limitation of output change with time results from internal or external frequency compensation capacitors slowing things down, which in turn results in delayed output changes with input changes. Limitations in slew rate capability can give rise to non-linear effects in electronic amplifiers. Slew rate is usually expressed in units of V/μs. The slew rate of OPAMP has to be very high for this particular application.[11]

*(2)* ***Input bias current*** – An OPAMP has infinite input resistance and therefore no input current. But in reality, however, small currents typically within Nano amperes to Pico amperes may be drawn by the inputs. The average of the currents entering

into the inverting and noninverting terminals of an OPAMP is referred to as input bias current .it has to be very low for getting expected performances.[11]

*(3)* ***Input offset voltage*** –In theory output voltage of an OPAMP should be zero when both inputs are zero. In reality, however a circuit imbalance within the internal circuitry can result in an output voltage. The input offset voltage is the voltage that must be applied between the input terminals of an OPAMP to nullify the output. The OPAMP chosen to work as an integrator should be of low input offset voltage.

## 1.1.2 Comparator

The comparator used in the system acts as a zero crossing detector. Zero crossing is the point of choice for measuring phase and frequency [3].The reference is usually easy to establish and the signals amplitude rate of change is maximum at signal zero. In alternating current, the zero-crossing is the instantaneous point at which there is no voltage present. A Zero Crossing Detector detects the transition of a signal waveform from positive and negative, ideally providing a narrow pulse that coincides exactly with the zero voltage condition. The zero crossing detector circuit is an important application of the op-amp comparator circuit. It can also be called as the sine to square wave converter. Anyone of the inverting or non-inverting comparators can be used as a zero-crossing detector. The only change to be brought in is the reference voltage with which the input voltage is to be compared, must be made. Selecting the proper comparator for the particular application appears to be difficult task, considering the thousands of comparators available currently on the market. The selection of comparator is based on following parameters:

*(1)* ***Response Time*** – It is the measure of how quickly a comparator changes output based on an input change. The response time is also referred as propagation delay in data sheets. The response time of the comparator should be very high to get desired response from the system.

*(2)* ***Hysteresis*** – Hysteresis is used to prevent noise from generating multiple zero crossings during the time that the measured signal is very close to zero. Inherently, the signal to noise ratio is the lowest at a zero crossing thus requiring large hysteresis voltages when high noise levels are expected.

*(3)* ***TTL compatible output*** –The output from comparator has to be TTL compatible to make it compatible with other system components especially ADC where output of ZCD is given to start of conversion pin of ADC.

## 1.1.3 Analog to Digital Converter

Selecting the proper ADC for a particular application appears to be a formidable task, considering the thousands of converters currently on the market. There are various factors to be considered for selecting ADC. These are listed as follows:

*(1)* ***Resolution-***It is the smallest change in the digital output that can be detected corresponding to a change in analog input. Higher the ADC resolution, better the time resolution for microseconds measurement. It is important to always design a system to allow for more bits than initially required. If an application calls for 12 bits of accuracy, choose a 16-bit converter.

*(2)* ***ADC Architecture*** Selecting the right ADC architecture is important as it decides the performance and successful implementation of the system to a great extent. Following are a few most widely used ADC architectures:

***Sigma Delta*** -For a wide variety of industrial measurement applications, the sigma-delta ADC is ideal; it is available in resolutions from 12 bits to 24 bits. Sigma-delta ADCs are suitable for a wide variety of sensor-conditioning, energy-monitoring, and motor-control applications.[9]

***Dual slope*** - This architecture is eliminates the power line noise of 50Hz / 60Hz and conversion time which is quite large.

***Flash*** – It is very fast: only 1 clock cycle per conversion. High complexity due to presence of $2^{B-1}$ comparators. Generally flash ADCs have a maximum resolution of 10 bits which is low. Our objective is to design a high resolution ADC. Flash ADCs are most commonly used in applications where only low resolutions are required. One of the key advantages of the Flash topology is that it has a potential latency of only one clock cycle – that is the digital output is available within one clock cycle.[2]

***Successive Approximation (SAR)*** – Successive approximation is the architecture of choice for nearly all multiplexed data acquisition systems, as well as many instrumentation applications. The SAR ADC is relatively easy to use, has no pipeline delay, and is available with resolutions to 18 bits and sampling rates up to 3 MSPS.The algorithm used in Successive Approximation is based on a binary search algorithm, and thus is more component efficient than Flash ADCs which use a brute force approach to perform data conversion. In a SAR ADC the analog input is sampled by a sample-and-hold circuit which operates at the effective Nyquist sampling rate of the

ADC, $f_s$. The significant advantage of the SAR ADC is that it uses only a few analog components (notably only a single comparator) to implement N-bit data conversion, resulting in a compact area and simple design. The SAR ADC allows for a significant reduction in the number of analog components it comes at the cost of restricting the maximum sampling rate to only a fraction of the maximum speed available by a given technology. SAR ADCs have traditionally been restricted to low to medium speed, and medium to high accuracy applications.[10][1]

*Pipelined* **ADC-** Pipelined ADCs are available today with resolutions of up to 14 bits and sampling rates over 100 MHz. They are ideal for many applications that require not only high sampling rates but high signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR).[1]
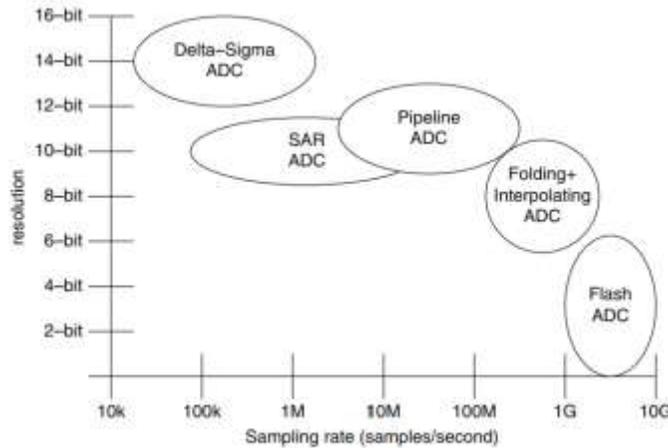


Fig 2.Comparison of ADC Architecture

## 1.1.4 Non-linearity

Non-linearity in the ADC may cause the actual curve to deviate slightly from the perfect curve. There are two major types of non-linearity that degrade the performance of ADC. They are differential non-linearity (DNL) and integral non-linearity (INL).[8]

*(1) Differential non-linearity (DNL) –* Differential non-linearity (DNL) is defined as the maximum and minimum difference in the step width between actual transfer function and the perfect transfer function. Non-linearity produces quantization steps with varying widths, some narrower and some wider as shown in Fig 3.
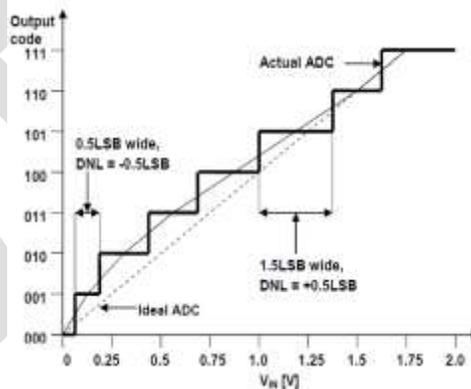


Fig 3.Plot showing the DNL

For the case of ideal ADC, the step width should be 1LSB. But an ADC with DNL shows step widths which are not exactly 1LSB. In Figure3, in a maximum case the width of the step with output value 101 is 1.5LSB which should be 1LSB. So the DNL in this case would be +0.5LSB.Whereas in a minimum case, the width of the step with output value 001 is only 0.5LSB which is 0.5LSB less than the expected width. So the DNL now would be 0.5LSB.

*(2) Integral non-linearity (INL) –* Integral non-linearity (INL) is defined as the maximum vertical difference between the actual and the ideal curve. It indicates the amount of deviation of the actual curve from the ideal transfer curve. INL can be interpreted as a sum of DNLs. For example several consecutive negative DNLs raise the actual curve above the ideal curve as shown in Figure 3 and the INL in this case would be positive. Negative INLs indicate that the actual curve is below the ideal curve. This means that the distribution of the DNLs determines the integral linearity of the ADC.
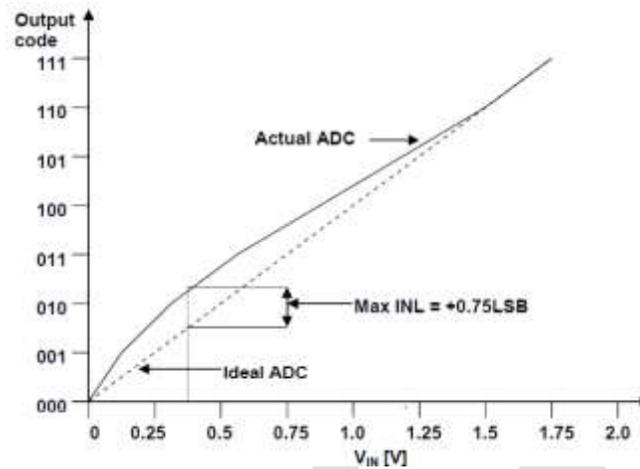


Fig 4.Plot showing the INL

The INL can be measured by connecting the midpoints of all output steps of actual ADC and finding the maximum deviation from the ideal curve in terms of LSBs. From the Figure 4, we can note that the maximum INL is +0.75LSB.

## 1.1.5 ADC timings

Basically an ADC takes some time for sampling and holding and for conversion.

*Sample and hold time-*Usually after giving a trigger to an ADC to start a conversion, it take some time (in clock cycles) to charge the internal capacitor to a stable value so that the conversion result is accurate. This time is called as sample time. After the sampling time, the number of clock cycles it takes to convert the charge or the voltage across the internal sampling capacitor into corresponding digital code is called the hold time.

*Conversion time-*Conversion time is the combination of the sampling time and the hold time, usually represented in number of clock cycles. The conversion time is the main parameter in deciding the speed of the ADC.

*Acquisition Time-*Acquisition time is the time required to charge and discharge the holding capacitor on the front end of an ADC.It is the maximum time required to acquire a new input voltage once a sample command has been given. (Hold to sample time) This parameter becomes crucial when the time difference between the inputs arriving at the same channel is extremely small.

*Aperture Delay-*Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the Convert input and when the input signal is held for a conversion.

*Aperture Jitter-*Aperture Jitter is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise. It results from the noise superimposed from the hold command and causes corresponding voltage error. It is usually measured in rms.

## TAC CHARACTERISTICS

The characteristic of TAC depends on the components involved in the operation. The characteristics of the TAC described as follows:

*(1) Linearity-*The property of linearity depend on the ramp produced by integrator is very important. Ramp generated has to be linear to enable proper time to amplitude conversion. Any change in the slope of ramp will lead to errors in the output voltage which represents Phase Shift. Linearity depends on current (I) flowing through integrator current (I) flowing through integrator where

$$I = I_{leakage} + I_{s/wleakage} + I_{bias}$$
$$I_{leakage} = \text{Leakage current of capacitor}$$

$I_{s/wleakage}$ = Leakage current of switch

$I_{bias}$ = Input bias current of OPAMP

*(2)* *Time Resolution-* The time resolution is the ability to distinguish between two time intervals with even the smallest change in the input time that can be reflected at the output voltage. The time resolution of system depends on ADC and range of time measurement. Hence, the TAC output range shall be compatible with ADC voltage range.

## TIMING DIAGRAM

The Fig 5 shows the main TAC signals. The TAC is a START-STOP type.

- By the arrival of the new START signal from ZCD of reference channel starts a ramp in integrator and the ramp output voltage is fixed at 5V.

- After the arrival of a start signal, any STOP signal from the ZCD of any of the four channel during which a output voltage corresponding to phase shift is obtained.

- When the rising edge of the STOP signal from ZCD reaches into ADC's start of conversion pin (soc), ADC acquire the instant voltage from the linearly rising ramp which represents the Phase Shift and is displayed on Personal Computer(PC)

- The conversion capacitor is discharged after a defined interval and the converter returns to the initial conditions, so that a new start signal can be accepted.
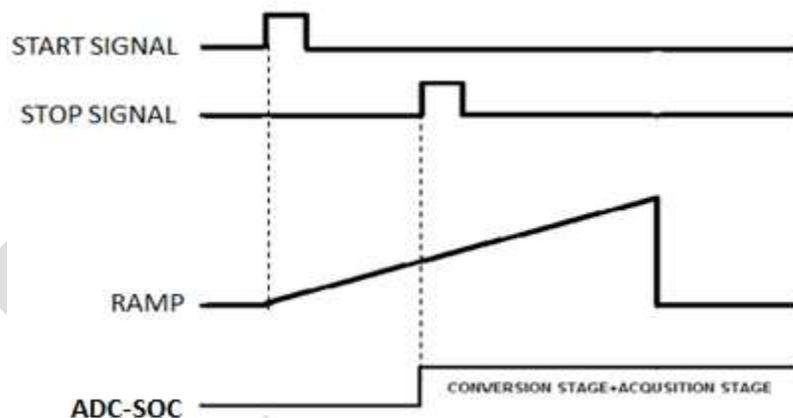


Fig 5.Timing Diagram of main TAC signals

## EXPERIMENTAL RESULTS

The designed converter has been experimentally characterized and the performance has been evaluated. The Fig 7&8 shows the output of individual circuits of the designed TAC. The integrator output is a linear ramp whose maximum voltage is 5V for duration of 8.6μs.The ZCD output shows the fast response of the comparator. The proper selection of components leads to the satisfactory response. The following table shows the set voltage value, calculated ADC count, and the obtained ADC count, the voltage obtained by scaling ADC count, and Percentage error of reading.

Fig.6 Experimental setup
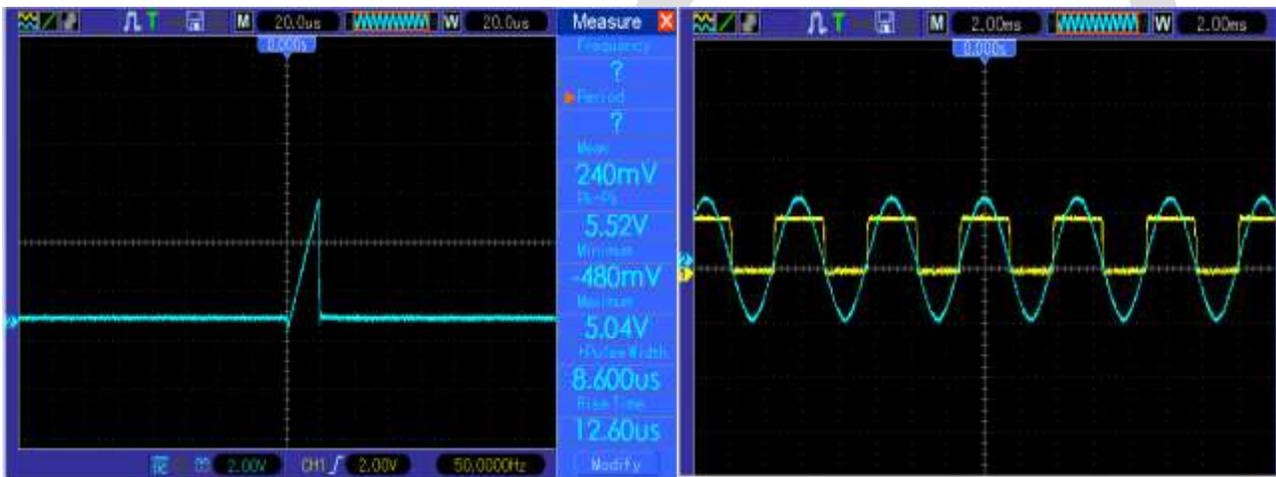


Fig.7Observed  output for Integrator and ZCD

| Sr.No | Set value | Calculated count | Obtained count | Obtained voltage | % Error reading |
|---|---|---|---|---|---|
| | V | | | V | % |
| 1 | 0.50492 | 6616 | 6616 | 0.5094 | 0.004 |
| 2 | 1.4999 | 19654 | 19655 | 1.49998 | -0.005 |
| 3 | 2.0001 | 26208 | 26211 | 2.0003 | -0.01 |
| 4 | 2.5 | 32759 | 32762 | 2.50025 | -0.011 |
| 5 | 3.0001 | 39312 | 39316 | 3.00042 | -0.011 |
| 6 | 3.5008 | 45873 | 45876 | 3.50113 | -0.009 |
| 7 | 4 | 52414 | 52416 | 4.00015 | -0.004 |
| 8 | 4.504 | 59018 | 59005 | 4.503 | 0.022 |
| 9 | 4.9954 | 65448 | 65452 | 4.99501 | -0.022 |

Fig.8 Observed output of ADC

## ACKNOWLEDGEMENT

## CONCLUSION

The results obtained from this high resolution system have very low percentage error. The designed circuit is implemented successfully for measurement of voltages (microvolts) in high resolution. The selected components like OPAMP, comparator and ADC are made to achieve expected output. The chosen ADC is capable to capture instantaneous data with a high resolution of 16 bits. TAC designed in this project is a measure of the distribution of time intervals between starts and stop pulses and is often referred to as "time range".

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