Switched Inductor Quadratic Buck Converter

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Abstract— A dc-dc converter featuring a steep step down of the input voltage is presented. The proposed converter uses two quadratic buck converters integrated with switched inductor structure. The structure formed by two inductors and two diodes is known as switched inductor structure. When the switch is on, the inductors are charged in series and when the switch is off, the inductors are discharged in parallel in switched inductor structure. The dc voltage conversion ratio of this converter has a quadratic dependency on duty cycle, providing a large step down. The stress voltage over the switches is reduced as compared to the quadratic buck converter. A complete theoretical analysis of the converter is done in continuous conduction mode. Also simulation results are presented which verify the theoretical analysis.

Keywords— quadratic, switched inductor, switch voltage stress, voltage conversion ratio

INTRODUCTION

The conventional buck converter whose voltage conversion ratio is the duty cycle, cannot provide a steep step-down of the line voltage, as required by modern applications. Certain applications such as microprocessors and on-board voltage regulators in PCs and laptops require very wide voltage step-down factor. The buck converter when integrated with switched inductor structure [2], high voltage conversion can be achieved. But the switch voltage stress is greater than input voltage. The buck quadratic PWM soft-single-switched (SSS) converter can provide a voltage conversion which have a quadratic dependency on duty cycle, but again switch stress is greater than input voltage [3]. The quadratic buck self-resonant (SR) PWM converter can achieve quadratic voltage gain and also switch stress is low [4]. But the number of switches is three and number of components is high.

The quadratic buck converter can achieve quadratic voltage gain and also one switch is used [5]-[7]. Here also switch voltage stress is high. Then double quadratic buck converter can achieve quadratic voltage gain and switch voltage stress is less than input voltage [1].

Double quadratic buck converter is shown in fig.1 [1]. The double quadratic buck converter is characterized by average output voltage to be lower than input voltage, and the voltage of intermediate capacitor also to be lower than the input voltage. Furthermore, it has high gain ratio compared to the conventional buck converter. In this structure, both the power supply and the intermediate capacitor will behave as voltage source. The load should behave as a current source and the current on the intermediate capacitor is given by the difference between the current across the inductor $L_1$ and the current in the switch $S_1$. Because of its symmetrical topology, the lower components have the same behavior of the respective upper component.

When switched inductor structure is combined with buck, buck-boost, Cuk, Sepic, Zeta converters to get a step down function. In this paper two quadratic buck converter are integrated with switched inductor structure to obtain a steep step down of the input voltage.
SWITCHED INDUCTOR QUADRATIC BUCK CONVERTER

The proposed converter is shown in fig.2. For symmetry, the value of inductors \( L_1 \) and \( L_4 \) are equal and also \( L_2 \) and \( L_3 \). Also, the capacitors \( C_1=C_2 \) and voltage across each capacitor is taken as \( V_c/2 \). When compared to double quadratic buck converter, the proposed converter uses only one source.

![Fig 2: switched inductor quadratic buck converter](image1)

PRINCIPLE OF OPERATION

Fig.2 shows the basic circuit diagram of the switched inductor quadratic buck converter in CCM. The inductors \( L_1, L_2 \) and diodes \( D_4, D_5 \) form the switched inductor structure. There are two stages of operation for this circuit.

![Fig 3: mode 1 operation](image2)

![Fig 4: Mode 2 operation](image3)
The equivalent circuit corresponding to stage 1 is shown in fig.3. During this interval, both the switches are ON. The input voltage \( V_1 \) appears in series across the inductors. The voltage across \( L_1 \) is given by

\[
v_{L1}(t) = \frac{V_1 - V_C}{2} = L_1 \frac{di_{L1}(t)}{dt}
\]

The current through \( L_1 \) is given by,

\[
i_{L1}(t) = \frac{1}{L_1} \int_0^t v_{L1}(t) \, dt = \frac{V_1 - V_C}{2L_1} (t) + i_{L1}(0).
\]

Where \( i_{L1}(0) \) is the initial current in the inductor \( L_1 \) at time \( t=0 \). The peak current through \( L_1 \) is

\[
i_{L1}(DT) = \frac{V_1 - V_C}{2L_1} DT + i_{L1}(0),
\]

And the peak to peak current of \( L_1 \) is

\[
\Delta i_{L1} = i_{L1}(DT) - i_{L1}(0) = \frac{V_1 - V_C}{2L_1} DT
\]

The voltage across inductor \( L_2 \) is given by

\[
v_{L2}(t) = \frac{V_C - V_0}{2} = L_2 \frac{di_{L2}(t)}{dt}
\]

Similarly,

The peak to peak current of \( L_2 \) is

\[
\Delta i_{L2} = i_{L2}(DT) - i_{L2}(0) = \frac{V_C - V_0}{2L_2} DT
\]

The equivalent circuit corresponding to stage2 is shown in fig.4. During this interval, both the switches are OFF. The inductor \( L_1 \) and \( L_4 \) begins to discharge through capacitors \( C_1 \) and \( C_2 \) respectively. The voltage across \( L_1 \) is given by

\[
v_{L1}(t) = \frac{-V_C}{2}
\]

The current through \( L_1 \) is given by,

\[
i_{L1}(t) = \frac{-V_C}{2L_1} (t - DT) + i_{L1}(DT),
\]

Where \( i_{L1}(DT) \) is the initial current in the inductor \( L_1 \) at time \( t=DT \). At time \( t = T \), the value of inductor current is

\[
i_{L1}(T) = \frac{-V_C}{2L_1} (T - DT) + i_{L1}(DT),
\]

Thus, the peak to peak current of \( L_1 \) is

\[
\Delta i_{L1} = i_{L1}(T) - i_{L1}(DT) = \frac{-V_C}{2L_1} T(1 - D)
\]

The voltage across inductor \( L_2 \) is given by

\[
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\]
Similarly, the peak to peak current of \( L_2 \) is

\[ \Delta i_{L2} = i_{L2}(T) - i_{L2}(DT) = \frac{V_0}{2L_2} T (1 - D) \]

CIRCUIT ANALYSIS

By the principle of volt-sec balance, the average steady state DC voltage across the inductor is zero. Let us first derive the voltage-time relation for \( L_1 \).

\[ \frac{V_1 - V_C}{2} DT + \frac{V_C}{2} (1 - D) T = 0 \]

Yielding,

\[ V_C = D V_1 \]

Similarly, applying volt-sec balance for \( L_2 \),

\[ \frac{V_C - V_0}{2} DT + (-V_0) (1 - D) T = 0 \]

Yielding,

\[ V_0 = \frac{D V_C}{2 - D} \]

Thus, voltage gain

\[ \frac{V_0}{V_1} = \frac{D^2}{2 - D} \]

The peak value of inductor current is given by,

\[ i_{L2}(DT) = \frac{(V_C - V_0)}{2L_2} DT + i_{L2}(0) \]

At boundary between continuous and discontinuous modes, the inductor current is zero, i.e., \( i_{L2}(0) = 0 \). Therefore, above eq. reduces to

\[ \Delta i_{L2} = i_{L2}(DT) = \frac{(V_C - V_0)}{2L_2} DT \]

Similarly,

\[ \Delta i_{L1} = i_{L1}(DT) = \frac{V_1 - V_C}{2L_1} DT \]

Since, the L-C filter networks are similar to the conventional buck stage, the equations for minimum values of filter capacitors can be obtained by similar methods.

\[ C_{omin} = \frac{(1 - D) V_0 T_s^2}{8L_2 \Delta V_C} \]

\[ C_{1min} = \frac{(1 - D) V_0 T_s^2}{8L_1 \Delta V_C} \]
SIMULATION RESULTS

The switched inductor quadratic buck converter with the following specifications is considered: \( V_1 = 400 \text{ V}, f_s = 50 \text{ kHz} \) and duty ratio, \( D = 0.5 \) and is constructed using MATLAB/Simulink simulator. The ripple voltage at the output is designed to be 1% of the average output voltage. The ripple current in the inductor is designed to be 10% of the total current, in continuous conduction mode. Using the design equations obtained in above section, the values of inductors and capacitors are found to be: \( L_1 = 8 \text{ mH}, L_2 = 0.866 \text{ mH}, C_0 = 1 \mu \text{F} \) and \( C_1 = 22 \mu \text{F} \). Fig. 5 shows the Simulink diagram of the proposed converter.

![Simulink model of switched inductor quadratic buck converter](image)

Gate pulse is given with a duty ratio of 50%. The gate pulse given to both the switches are same and is shown in fig. 6. The voltage stress across the switch is measured to be 300V and is shown in fig. 7. The output voltage is shown in fig. 8 and is measured to be 66V.

![Gate pulse to switch](image)

**Fig 6: Gate pulse to switch**

![Voltage across the switch](image)

**Fig 7: Voltage across the switch**

![Output Voltage](image)

**Fig 8: Output Voltage**

Then the performance analysis of four converters is done. The performance comparison is done with following parameters: Input voltage=400V, switching frequency=50 kHz, Duty Cycle=50%. The performance is summarized in the following table.
Table 1: Comparison of topologies

<table>
<thead>
<tr>
<th>Converter Type</th>
<th>Output Voltage(V)</th>
<th>Switch Voltage(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional Buck Converter</td>
<td>200</td>
<td>400</td>
</tr>
<tr>
<td>Quadratic Buck Converter</td>
<td>100</td>
<td>600</td>
</tr>
<tr>
<td>Double Quadratic Buck Converter</td>
<td>100</td>
<td>300</td>
</tr>
<tr>
<td>Switched Inductor Quadratic Buck Converter</td>
<td>66</td>
<td>300</td>
</tr>
</tbody>
</table>

From the table it can be seen that when switched inductor quadratic buck converter is used high voltage conversion can be achieved with less switch voltage stress.

CONCLUSIONS

The study of switched inductor quadratic buck converter is presented in this paper. The stages of operation and circuit analysis of the proposed converter is done in continuous conduction mode. Simulation results are presented for continuous conduction mode and show low value in the output voltage over the input voltage, providing the high conversion rate of the converter. With the help of proposed converter, high switching frequencies can be obtained. From the above table, it can be seen that switched inductor quadratic buck converter can provide steep step down of the voltage and reduced switch voltage stress can be obtained.

REFERENCES:


