A Strategical Description of Ripple Borrow Subtractor in Different Logic Styles

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ABSTRACT – The demand and popularity of portable electronics is driving designers to strive for small silicon area, higher speeds, low power dissipation and reliability. Design of 2-input AND, 2-input OR, 2-input XOR and an INVERTER, which are the basic building blocks for the 4-bit Ripple borrow subtractor. This paper thoroughly involves designing of ripple borrow subtractor in cMOS logic, transmission gate logic and pass transistor logic styles. The schematic design is further transferred to prefabrication layout. Simulation of the microwind layout realizations of the subtractor is performed and results are discussed. From the results obtained comparison of cMOS logic, transmission gate logic and pass transistor logic is done and discussing the efficient logic for ripple borrow subtractor.

Keywords – cMOS logic, transmission gate logic, pass transistor logic, full subtractor, ripple borrow subtractor.

INTRODUCTION

In this paper, we have presented a brief review on Ripple borrow subtractor using cMOS, transmission gates and pass transistor logic style. The basic circuit diagram of 1 bit Full subtractor is as described below along with the block diagram and its truth table. Full subtractor is a combinational circuit which is used to perform subtraction of three bits, it has three inputs a(minuend) and b(subtrahend) and borrow_in(subtrahend) and two outputs d(difference) and borrow_out(borrow).

Fig. 1. Gate level representation of full subtractor

Fig. 2. Truth table and block diagram of full subtractor
CIRCUIT TECHNIQUES

FULLSUBTRACTOR

The full-subtractor circuit subtracts three one-bit binary numbers (A, B, borrow_in) and outputs two one-bit binary numbers: a difference (D) and a borrow (borrow_out).

RIPPLE BORROW SUBTRACTOR

It is possible to create a logical circuit using multiple full subtractors to subtract N (precise 4-bit numbers). Each full subtractor inputs a borrow_in (borrow input) which is the borrow_out (borrow output) of the previous subtractor. This kind of subtractor is ripple borrow subtractors since each borrow bit ripples to the next full subtractor.

4-BIT RIPPLE BORROW SUBTRACTOR USING CMOS CIRCUITS

CMOS is referred to as complementary-symmetry metal-oxide semiconductor (COS-MOS). The words “complementary-symmetry” refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. The circuit level description of the Ripple Borrow Subtractor in CMOS logic is described below.
4-BIT RIPPLEBORROW SUBTRACTOR USING TRANSMISSIONGATES

The CMOStransmissiongategate consists of two MOSFETs, one n-channel responsible for correct transmission of logic low, and one p-channel, responsible for correct transmission of logic high. The circuit level description of the Ripple Borrow Subtractor in Transmission Gate logic is described below.

![Image of Ripple Borrow Subtractor in Transmission Gate Logic](image1)

**Fig. 3.** Ripple Borrow Subtractor in Transmission Gate Logic.

4-BIT RIPPLEBORROW SUBTRACTOR USING PASS TRANSISTORS

We can view the complementary CMOS gate as switching the output pin to one of power or ground. A slightly more general gate is obtained by fusing switches to output pin to one of power; ground; or any of the input signals. In such designs, the MOSFETs considered to be a pass transistor. When used as a pass transistor, the device may conduct current in either direction. The circuit level description of the Ripple Borrow Subtractor in Pass Transistor logic is described below.

**From full subtractor truth table**

<table>
<thead>
<tr>
<th>Diff</th>
<th>Bc</th>
<th>Bc</th>
<th>Bc</th>
<th>Bc</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>A</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
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<td>A</td>
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<tr>
<td>A</td>
<td>0</td>
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<td>3</td>
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<tr>
<td>A</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
</tr>
<tr>
<td>A</td>
<td>9</td>
<td>A</td>
<td>A</td>
<td>1</td>
</tr>
</tbody>
</table>

![Image of Ripple Borrow Subtractor in Transmission Gate Logic](image2)

**Fig. 4.** Ripple Borrow Subtractor in Transmission Gate Logic.

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DESIGN AND LAYOUT ASPECTS

LAYOUT OF RIPPLE BORROW SUBTRACTOR USING CMOS LOGIC

![Layout of ripple borrow subtractor using CMOS logic](image1)

Fig. 5. Layout of ripple borrow subtractor using CMOS logic

LAYOUT OF RIPPLE BORROW SUBTRACTOR USING TRANSMISSION GATE LOGIC

![Layout of ripple borrow subtractor using transmission gate logic](image2)

Fig. 6. Layout of ripple borrow subtractor using transmission gate logic

LAYOUT OF RIPPLE BORROW SUBTRACTOR USING PASS TRANSISTOR LOGIC

![Layout of ripple borrow subtractor using pass transistor logic](image3)

Fig. 7. Layout of ripple borrow subtractor using pass transistor logic

SIMULATION AND RESULTS

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SIMULATION OF RIPPLE BORROW SUBTRACTOR USING CMOS LOGIC

![Diagram of CMOS logic simulation](image1)

Fig. 8. Simulation of ripple borrow subtractor using CMOS logic

SIMULATION OF RIPPLE BORROW SUBTRACTOR USING TRANSMISSION GATE LOGIC

![Diagram of transmission gate logic simulation](image2)

Fig. 9. Simulation of ripple borrow subtractor using transmission gate logic

LAYOUT OF RIPPLE BORROW SUBTRACTOR USING PASS TRANSISTOR LOGIC

![Diagram of pass transistor logic layout](image3)

Fig. 10. Simulation of ripple borrow subtractor using pass transistor logic
POWER ANALYSIS

The table shows the results of 4-bit ripple borrow subtractors using CMOS circuits. Transmission gates and Pass Transistors. It compares these circuits regarding Power consumption. Fig. 11 represents the above results graphically.

![Power Consumption Chart]

Fig. 11. Power consumption.

CONCLUSION

In this paper, an attempt has been made to design 2-input AND, 2-input OR, 2-input XOR, which are the basic building blocks for the benchmark circuits 4-bit Ripple borrow subtractor. The proposed circuits have offered an improved performance in power dissipation. In this paper, we can be concluded that the power dissipation of transmission gate circuits is much lesser than the power dissipation of CMOS and Pass transistors, thus it proves to be more efficient than the circuits from CMOS and Pass transistors. The circuit and its VLSI technology is very useful in the applications related to rural development as it is less power consuming and thus can be efficiently used in various technologies.

REFERENCES:


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